David Jorge Tiago Amoêdo

Licenciatura em Engenharia Eletrotécnica e de computadores

A 1.2 V Low Noise Amplifier with Double Feedback for High Gain and Low Noise Figure

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Orientador: Prof. Doutor Luís Augusto Bica Gomes de Oliveira, FCT-UNL

Júri:

Presidente: Prof. Doutor Paulo Miguel de Araújo Borges Montezuma de Carvalho, FCT/UNL
Arguente: Prof. Doutor João Pedro Abreu de Oliveira, FCT/UNL
Vogal: Prof. Doutor Luís Augusto Bica Gomes de Oliveira,

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

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I dedicate this thesis to my family, mainly to my father Rui Amoêdo, to my mother Fernanda Amoêdo, to my sister Catarina Amoêdo, to my grandmother Ercilia Mendes and all the rest of people that are importants to me.

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Universidade Nova de Lisboa

Abstract

Faculdade de Ciências e Tecnologia

Departamento de Engenharia Eletrotécnica e de Computadores

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

por David Jorge Tiago Amoêdo

In this thesis we present a balun low noise amplifier (LNA) in which the gain is boosted using a double feedback structure. The circuit is based in a Balun LNA with noise and distortion cancellation. The LNA is based in two basic stages: common-gate (CG) and common-source (CS). We propose to replace the resistors by active loads, which have two inputs that will be used to provide the feedback (in the CG and CS stages). This proposed methodology will boost the gain and reduce the NF (Noise Figure). Simulation results, with a 130 nm CMOS technology, show that the gain is 19.65 dB and the NF is less than 2.17 dB. The total power dissipation is only 5 mW (since no extra blocks are required), leading to an FOM (Figure of Merit) of 3.13 mW^{-1} from a nominal 1.2 supply.

Universidade Nova de Lisboa

Resumo

Faculdade de Ciências e Tecnologia

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Nesta tese apresentamos um amplificador de baixo ruído (LNA), em que o ganho é aumentado através de uma estrutura double feedback. O circuito é baseado num Balun LNA com cancelamento de ruído e de distorção. O LNA é baseado em dois andares básicos: common-gate (CG) e common-source (CS). Propomo-nos a substituir as resistências por cargas ativas, que têm duas entradas que serão usados para fazer o feedback (nos andares CG e CS). Esta metodologia proposta vai aumentar o ganho e reduzir a NF. Os resultados de simulação, com uma tecnologia CMOS de 130 nm, mostra que o ganho é de 19,65 dB e o NF é inferior a 2,17 dB. A dissipação de energia total é de apenas 5 mW (uma vez que não são necessários blocos adicionais), obtendo uma FOM de 3.13 mW-1 a partir de uma tensão de entrada de 1,2 V.

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Abbreviations

AC	**A**lternating **C**urrent
CG	**C**ommon **G**ate
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CS	**C**ommon **S**ource
DC	**D**irect **C**urrent
ISM	**I**ndustrial **S**cientific and **M**edical
IIP	**I**nput Referred **I**nterception **P**oint
GPS	**G**lobal **P**osition **S**ystem
LNA	**L**ow **N**oise **A**mplifier
LO	**L**ocal **O**scillator
LOM	**L**NA **O**scillator **M**ixer
NF	**N**oise **F**actor
NMOS	**N**channel **M**etal-**O**xide-**S**emiconductor
PMOS	**P**channel **M**etal-**O**xide-**S**emiconductor
Q	**Q**uality factor
RF	**R**adio **F**requency
VCO	**V**oltage **C**ontroller **O**scillator
FOM	**F**igure **O**f **M**erit
ADC	**A**nalog to **D**igital **C**onverter
DSP	**D**igital **S**ignal **P**rocessor
SNR	**S**ignal to **N**oise **R**atio
QPSK	**Q**uadrature **P**hase-**S**hift **K**eying
BER	**B**it **E**rror **R**ating
AM	**A**mplitude **M**odulation
RC	**R**adio **C**ontrolled
WMTS	**W**ireless **M**edical **T**elemetry **S**ervice

Chapter 1

1 Introduction

1.1 Background and Motivation

The technology and electronic devices have started to have a big impact in society. Many companies had to develop and improve their systems, reducing cost and power consumption to can compete in many fronts and in many economic markets. Several sectors of society such as medicine, video games industry, telecommunications services and areas related with microchips and computers were crucial for the growing of electronic, as well as all the techniques used to support that maturity.

The low voltage and low consumption electronic systems are needed and they are the preferential demand in industry. This reality has more and more impact in all firms, workers and mainly in the consumers around the world.

Nowadays, there is a high demand for wireless communications, which includes Industrial, Scientific, and Medical (ISM) and Wireless Medical Telemetry Service (WMTS) applications [1]. These low cost applications require low power, low voltage transceivers fully integrated in a single chip [2, 3]. The LNA that is a key block in these systems will be investigated in this thesis and they may be divided into two groups: narrowband LNA and wideband LNA.

- ✓ Narrowband LNAs use inductors and have very low noise figure, but they use a large area and require a technology with RF options to have inductors with high Q.
- ✓ Wideband LNAs with multiple narrowband inputs have low noise, but their design is very complicated and the area and cost are high [2, 4].

RC LNAs are very simple wideband, but the conventional topologies have large noise figures. Recently, wideband LNAs with noise and distortion cancelling [5] have been proposed, which may have noise figures below 3 dB. Inductorless circuits have reduced die area and cost [6].

Wideband LNAs with high gain and low noise figure (NF), using noise and distortion cancelation have been proposed [5-7]. But, these circuits have large power dissipation for high gain and low noise figure.

In this thesis, the main goal is to design a very low area and low cost LNA, with very high gain and low NF using a 1.2 V supply. This is obtained by replacing the load resistors by transistors biased close to saturation. In [7] a circuit operating at 1.2 V with controllable gain was proposed. In

this thesis, is investigated the possibility of introduce a double feedback technique to boost the gain and reduce the noise figure.

1.2 Thesis Organization

This thesis has been organized in six chapters, including this introduction.

In Chapter 2 are done some descriptions of the principal receiver's topologies, as well as for the principal receiver block, the LNA. After this, is described the existing LNA topologies, doing a distinction between inductor and inductorless LNAs. Is also introduced the definitions, the basic concepts and figures of merit, which are employed in LNAs.

In Chapter 3 is done a briefly description of the common-gate (CG) and the common-source (CS) stages, which are used in the proposed LNA of this thesis.

In Chapter 4 is presented the LNA structure which combines the two amplifiers stages. The principle of noise cancelation is explained and it is shown some different examples of this technique.

In Chapter 5 is investigated a Double Feedback structure, which is the proposed circuit in this thesis. A theoretical analyses is made to obtain the equations of the circuit in order to optimize the circuit. It is also shown the simulations results of the optimized design. The circuit layout is produced and are shown the post-simulations results. Comparison with the state-of-the-art wideband LNAs is made.

Finally, in Chapter 6 is given the overall conclusions and further research suggestions.

1.3 Contributions

For the complete LNA (combined CG and CS balun topology) is compared the conventional design (with resistors) with the new MOSFET-Only with Double Feedback implementation optimized for Gain and Noise Figure (NF).

In this work, equations of gain are presented, which can be used to optimize the circuit performance. A circuit prototype in 130 nm standard CMOS technology at 1.2 V have been designed and simulated to demonstrate the proposed technique. Finally, we are presented all the simulation results of gain and NF before and after the layout.

This work has originated the paper at the 4th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS'13). It was developed directly related with the main goal of this work entitled "A 1.2 V Low Noise Amplifier with Double Feedback for High Gain and Low Noise Figure".

Chapter 2

2 State-of-the Art Receiver Architectures and LNAs

In the present chapter, receiver architectures and the main RF (radio frequency) front-end blocks are presented.

A transmitter, a receiver and a communication channel, in which the transmitted signals propagate, are the key blocks of a communication system. In the case of wireless systems, the information that is sent by the transmitter is included in a RF signal via a modulation process, i.e. by varying at least one of the signal's characteristics (amplitude, frequency or phase). Upon arrival at the receiver, the information needs to be recovered from the original RF signal through a demodulation process. The communication medium, namely air (in the case of wireless communications), is not ideal since the signals received are typically very weak (~ microvolts) and are susceptible to suffer interference from other, possibly stronger, signals. It is therefore important to be able to eliminate undesired signals and isolate the signal of interest, so that it can be later amplified and converted to baseband to go through demodulation, allowing the information contained in the signal to be recovered.

2.1 Receivers Architectures

In order to carry more information in a signal, the signals are converted to high frequency for transmission and then converted back for the baseband for reception. The size of the antenna is also dependent on the frequency of the transmitted signal. Since the size is typically proportional to the wavelength of the signal, the required antennas are smaller. Unfortunately, the influence of parasitics (impedances, capacitors, etc.) is higher at high frequencies. The main receivers architectures commonly used today are described below [2-8].

2.1.1 Heterodyne Receiver

The super-heterodyne receiver topology (Fig. 2.1), proposed by U.S. Army Major Edwin Armstrong [9], is one of the most used architectures in wireless communication systems. The antenna receives the RF signal which is filtered by a bandpass filter and subsequently amplified by a low noise amplifier (LNA) and down-converted to a lower, intermediate frequency (IF) by a signal multiplier

(mixer), having the output of a local oscillator (LO) applied to it. In order to isolate the desired signal from signals present in adjacent channels, there is a bandpass filter at the desired frequency (IF), called the channel selection filter, at the mixer output.

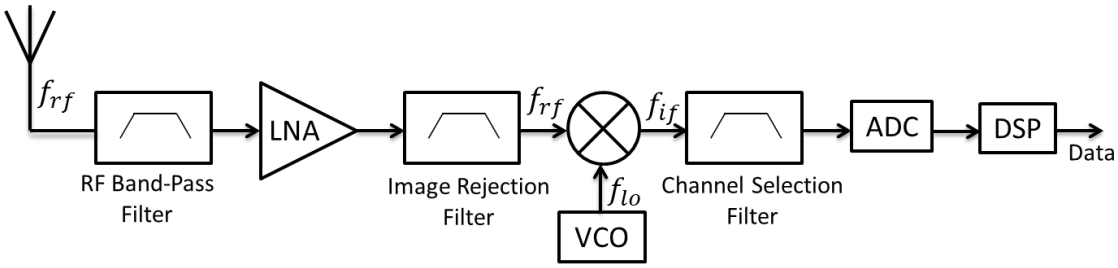

Figure 2.1- Super-Heterodyne Receiver.

Having IF, the desired RF frequency selected by tuning the LO, fixed is the major advantage of this architecture, since designing the filter, which should be very selective and have a high quality factor (Q), becomes much easier. Given that the process of demodulation takes place in the digital domain, the introduction of an analog to digital converter (ADC) becomes necessary, followed by a digital signal processor (DSP) to perform the demodulation process.

In order to gain a better understanding of the operation principle behind this receiver, namely regarding the mixing, let us consider that at the mixer inputs there are the RF and LO signals, given by

$$v_{rf}(t) = V_{rf}\, cos(\omega_{rf} t) \tag{2.1}$$

$$v_{lo}(t) = V_{lo}\, cos(\omega_{lo} t) \tag{2.2}$$

We obtain at the mixer output

$$v_{if}(t) = v_{rf}(t) v_{lo}(t) = \frac{1}{2} V_{rf} V_{lo} \left[cos\left((\omega_{rf} - \omega_{lo}) t \right) + cos((\omega_{rf} + \omega_{lo}) t) \right] \tag{2.3}$$

The wanted signal is the one with the lower frequency so, from (2.3), the desired frequency, given that $\omega = 2\pi f$, is

$$\omega_{if} = \omega_{rf} - \omega_{lo} \tag{2.4}$$

In the presented example, the local oscillator frequency is smaller than the desired frequency and this is called low-side injection. However, if the local oscillator frequency is higher, then it is called high-side injection and we obtain $\omega_{if} = \omega_{lo} - \omega_{rf}$.

A bandpass filter, centered on the IF (f_{if}), is used for channel selection, eliminating other unwanted signals that may appear in the spectrum. This process may present a challenge if, at the mixer input, there is an image signal, *i.e.* a signal with frequency $f_{im} = 2f_{lo} - f_{rf}$ (Fig. 2.2). From this signal, after multiplication, two signals with frequencies $f_1 = f_{lo} - f_{rf}$ and $f_2 = 3f_o - f_{rf}$ are originated, f_1 being coincident with f_{if}, overlapping the signal of interest and making it impossible to separate both signals. A filter, called image rejection filter, is therefore needed before the mixer to prevent the interference of the image signal.

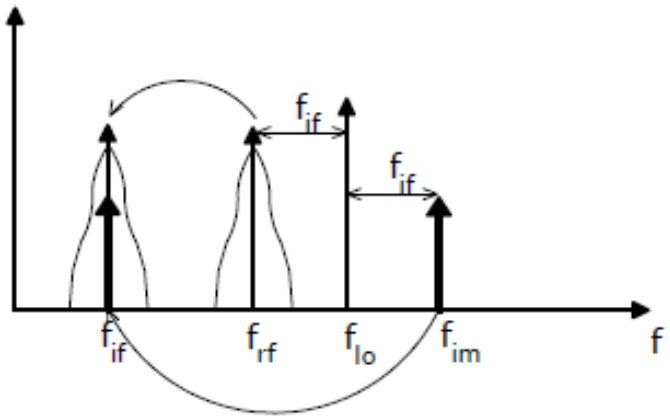

Figure 2.2 – Frequency spectrum showing the image signal adopted from [10].

The difference between the frequency of the RF and image signals is $2f_{if}$. Increasing f_{if} allows for the image rejection filter specifications to be less strict but at the same time, with the increase of f_{if} the channel selection filter is required to have tighter specifications for the same bandwidth due to the increase of the quality factor $Q = \frac{f_0}{\Delta f}$. A compromise between intermediate frequency and quality factor must be reached due to the difficulties present in the realization of filters with high Q with CMOS technology. In practice, high performance filters must be realized externally, rendering on chip full integration impractical.

2.1.2 Homodyne Receiver

Given the problems associated with the integration of the heterodyne receiver, another receiver topology, known as homodyne, direct conversion or "Zero-IF", can be used. This type of receivers can work in direct conversion configuration (Fig. 2.3 (a)) or in quadrature conversion (Fig. 2.3 (b)).

In the direct conversion receiver, the RF signal is translated to the baseband in a single down-conversion by using a LO with the same frequency as the RF signal. The resulting signal is then

filtered with a low-pass filter, which is simpler to design and integrate, in order to select the desired channel [2-3]. Given that the signal and its image are separated by $2f_{if}$, this zero *IF* approach implies that the desired channel is its own image and therefore the image rejection filter is no longer required. All the necessary processing is performed at the baseband and the requirements for the filters and ADC's are the more relaxed possible, favoring its integration [6].

Using modern modulation schemes, the signals are modulated in phase or frequency, which differs from amplitude modulation (AM) where the sidebands have the same information, and the down-conversion requires accurate quadrature signals [6]. Hence, in these cases, receivers with quadrature down-conversion are used in order to ensure the preservation of the information contained in the sidebands [10].

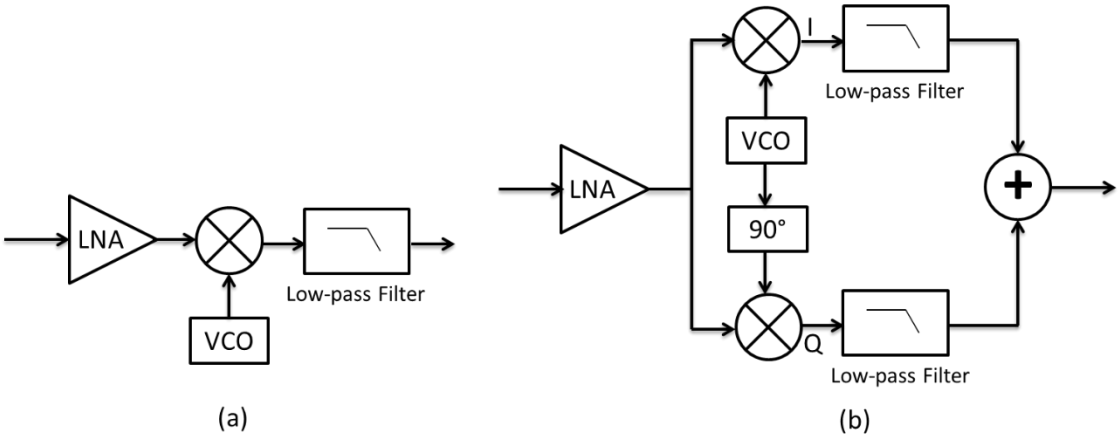

Figure 2.3 – Homodyne receiver: (a) single; (b) in quadrature adopted from [10].

Despite its simplicity, homodyne receivers present some drawbacks when compared with heterodyne receivers, which hinder the use of this architecture in more demanding applications. These disadvantages are explored below:

DC offsets – Given that the down-converted band extends down to zero frequency, the presence of any offset voltage can corrupt the signal and saturate the receiver's baseband output stages. This problem can originate in leakages between the LO port and the LNA and mixer inputs if the ports are not properly isolated, due to substrate and capacitive coupling. When a leakage signal "LO leakage" appears at the inputs of LNA and mixer, the result of this "self-mixing" is a DC component at the mixer output which can lead to saturation of the following components (Fig. 2.4 (a)). Similar effects occur if the leakage comes from the LNA or mixer input to the LO port of the mixer (Fig. 2.4 (b)).

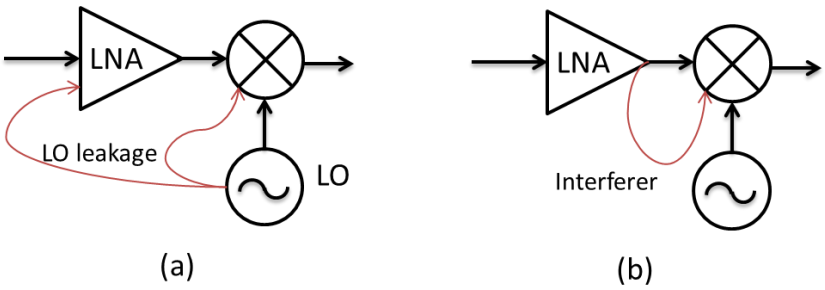

Figure 2.4 – DC offsets caused by "self-mixing": (a) "LO leakage"; (b) interferer.

Quadrature error – When dealing with frequency or phase modulation, quadrature signals are required, as explained earlier and ideally they should have the same amplitude and a phase shift of 90°. However, real circuits are not ideal and imbalances between I and Q appear, expressed as gain and phase errors. The result of "I/Q mismatch" is the corruption of the down-converted signal constellation and a consequent increase of the bit error rate (BER). This is the most critical aspect of these receivers, since modern wireless communication systems have different information in I and Q and the implementation of accurate high frequency components with very accurate quadrature relationship presents many challenges.

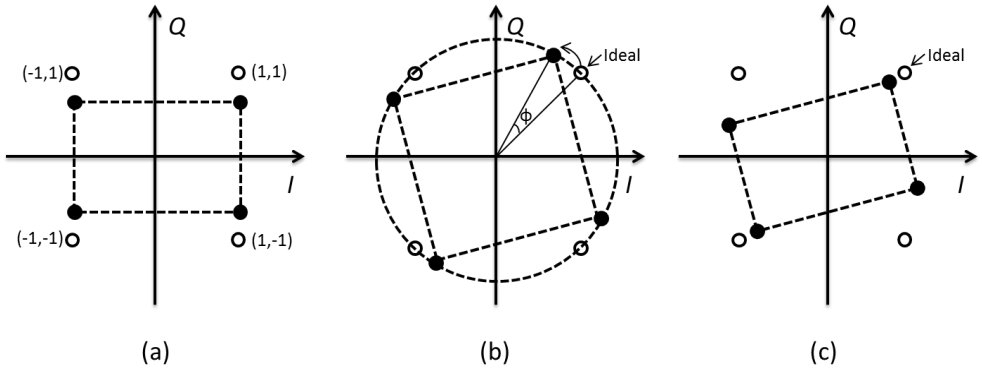

Figure 2.5 – Effect of I/Q mismatch in QPSK: (a) gain error, (b) phase error, (c) gain and phase error.

As example of the effect of I/Q mismatch on a Quadrature Phase-Shift Key (QPSK) constellation in presented in Fig. 2.4. If the Q path in the mixer has smaller conversion gain than the one for the I path, the Q signal will exhibit smaller amplitude than expected creating a gain error (Fig. 2.5(a)). Let us now assume that no gain error occurs but instead there is a phase error between the signals fed by the LO to the splitter

$$x_{LO,I}(t) = 2\,cos(\omega_0 t) \tag{2.5}$$

$$x_{LO,Q}(t) = 2\,cos(\omega_0 t + \phi) \tag{2.6}$$[1]

[1] The factor 2 present in equations (2.5) and (2.6) is merely present simplify the equations.

If the RF signal provided by the LNA is given by $x(t) = a\,cos(\omega_0 t) + b\,sin(\omega_0 t)$, with a and b equal to 1 or -1 to create the four constellation symbols, at the mixer output the following signals are obtained

$$y_I(t) = a + a\,cos(2\omega_0 t) + b\,sin(2\omega_0 t) \quad (2.7)$$

$$y_Q(t) = a + a\,sin(\phi) + b\,cos(\phi) + a\,sin(2\omega_0 t + \phi) - b\,cos(2\omega_0 t) \quad (2.8)$$

which are then added and passed by a low-pass filter giving a resulting signal at baseband given by

$$y(t) = y_I(t) + y_Q(t) = a + a\,sin(\phi) + b\,cos(\phi) \quad (2.9)$$

This result is directly related with the phase error illustrated in Fig. 2.5 (b). The combination of gain and phase error is exemplified in Fig. 2.5 (c).

Even order distortion – if the LNA has a second order nonlinearity, such as $y(t) = a\,x(t) + b\,x^2(t)$, and if near the channel of interest two interferers are present, $x(t) = A_1\,cos(\omega_1 t) + A_2\,cos(\omega_2 t)$ are present, then one of the resulting output terms will be given by $b\,A_1 A_2\,cos((\omega_1 - \omega_2)t)$ and this shows that one of the interferer component is close to the baseband $(\omega_1 - \omega_2)$. While in the case of ideal mixers this presents no problem, since this component becomes shifted to higher frequencies after multiplication by the LO signal, in the case of real mixers some feedthrough directly to the output will be present and part of the interferer will appear at the output at the baseband, distorting the signal (Fig. 2.6).

In order to avoid this drawback, differential LNA's and mixers are required to remove even order harmonics. However, this implies higher power consumption and larger circuit areas.

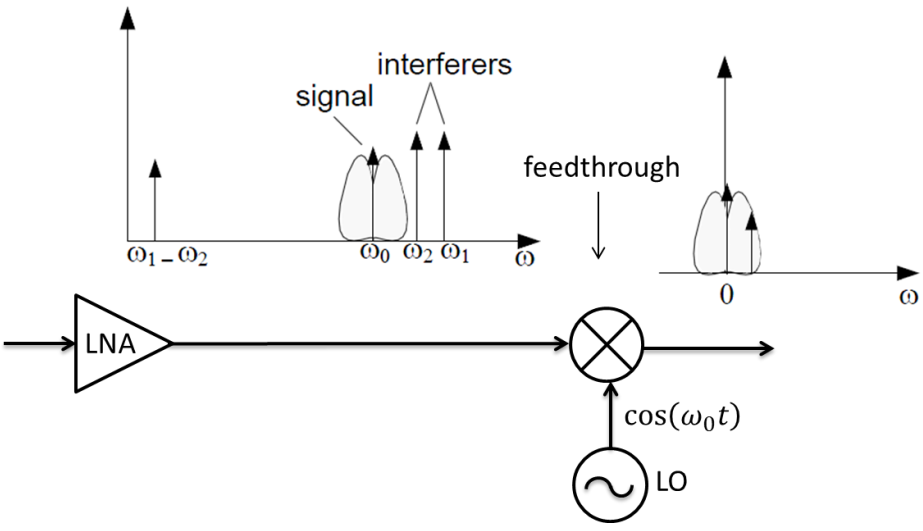

Figure 2.6 – Effect of even order distortion adopted from [10].

Flicker noise – Another problem in this architecture is the presence of "flicker noise" that, especially for MOSFET, is more relevant for low frequencies and it can substantially corrupt low frequency baseband signals. This topic will be subject to further discussion in a subsequent section dedicated to noise.

Despite its simplicity, this topology becomes impractical for certain applications, although there are solutions to the problems stated above by adding additional complexity to the circuit.

2.1.3 Low-IF Receiver

The low-IF topology is a solution that combines features from both types of receivers, heterodyne and homodyne, by using a mixed approach, *i.e.* by the selection of an intermediate frequency. This choice of frequency allows for the specifications of the channel selection filter to be relaxed while simultaneously avoids the problems related with direct conversion, especially the flicker noise, which, as state above, has a strong impact in the baseband signal. The image cancelation, which is a problem associated with heterodyne receivers, is achieved by using quadrature architectures, in which the image is suppressed after the generation of a negative replica.

Image cancelation techniques were proposed by Hartley [11] and Weaver [12]. Note that there are other architectures but we only speak about these two architectures.

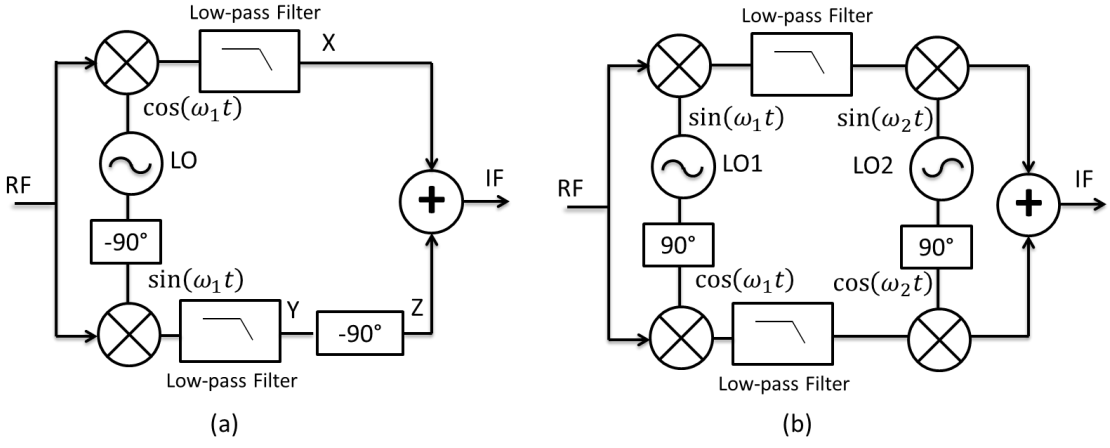

Figure 2.7 – Image rejection architectures: (a) Hartley; (b) Weaver.

The Hartley architecture is represented in Fig. 2.7 (a). Let us assume that

$$x_{RF}(t) = V_{RF}\, cos(\omega_{RF} t) + V_{IM}\, cos(\omega_{IM} t) \tag{2.10}$$

where V_{RF} and V_{IM} correspond, respectively, to the amplitude of the RF and image signals and ω_{IM} is the image frequency. After down-conversion and filtering the resulting signals at X and Y are

$$x_X(t) = \frac{V_{RF}}{2}\cos((\omega_{RF} - \omega_{LO})t) + \frac{V_{IM}}{2}\cos((\omega_{LO} - \omega_{IM})t) \quad (2.11)$$

$$x_Y(t) = -\frac{V_{RF}}{2}\sin\big((\omega_{RF} - \omega_{LO})t\big) + \frac{V_{IM}}{2}\sin((\omega_{LO} - \omega_{IM})t) \quad (2.12)$$

Given that $sin\left(\theta - \frac{\pi}{2}\right) = -cos\,\theta$, after a shift of -90°, at Z we obtain

$$x_Z(t) = \frac{V_{RF}}{2}\cos((\omega_{RF} - \omega_{LO})t) - \frac{V_{IM}}{2}\cos((\omega_{LO} - \omega_{IM})t) \quad (2.13)$$

In the last step of this procedure, the signals x_X and x_Z are added allowing the recovering of the desired signal while at the same time canceling the image component.

The Weaver architecture (Fig. 2.7(b)) is similar to the Hartley architecture, except the -90° phase shift in one of the signal paths is replaced by a second mixing operation in both signal paths, which has the same effect as the -90° phase shift used in Hartley's configuration. Direct conversion to the baseband can be achieved by adequately selecting the second LO frequency.

Despite the fact that both architectures of low-IF topology, Hartley and Weaver, are susceptible to I/Q mismatch which may lead to incomplete image rejection, it is still a flexible compromise between heterodyne and Zero-IF topologies.

2.2 Signal propagation

2.2.1 Impedance matching

In circuits that use high frequencies, the wavelengths tend to be of the same order of magnitude as the physical dimensions of the circuit. Therefore, lumped circuit analysis, which assumes nearly instantaneous signal propagation ($l_{circuit} \ll \lambda$), is not appropriate. In this scenario, circuit paths behave like transmission lines, which require distributed parameters analysis.

A segment of a transmission line can be represented by an equivalent lumped circuit (Fig. 2.8) [13]. The units R, G, L and C are defined per unit length throughout the text.

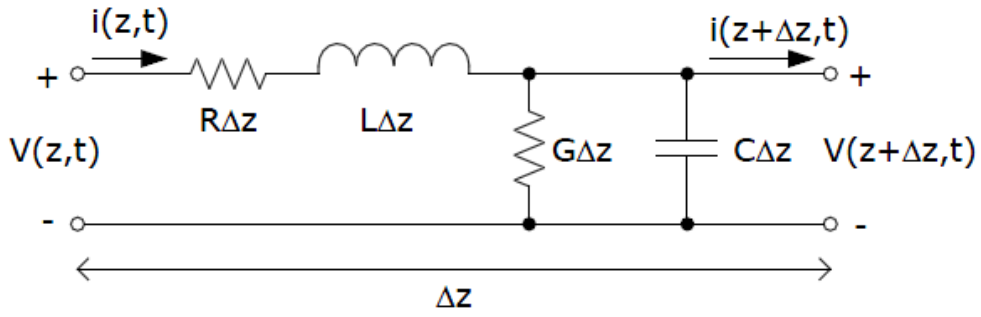

Figure 2.8 – Lumped circuit equivalent of a transmission line adopted from [10].

The resistance R represents the conductor loss while the conductance G is related to the dielectric loss between the two conductors. Given that we can represent the system as an equivalent lumped circuit, the Kirchhoff's voltage and current laws are applicable and we obtain

$$v(z,t) - R\Delta z\, i(z,t) - L\Delta z\, \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \tag{2.14}$$

$$i(z,t) - G\Delta z\, v(z+\Delta z,t) - C\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0 \tag{2.15}$$

Dividing both equations by Δz, taking the limit for $\Delta z \to 0$ and keeping in mind that the definition for the derivate of a function f is given by $f'(a) = \lim_{\Delta x \to 0} \frac{f(a+\Delta x)-f(a)}{\Delta x}$, the result gives:

$$\frac{\partial v(z,t)}{\partial z} = -R\, i(z,t) - L\frac{\partial i(z,t)}{\partial t} \tag{2.16}$$

$$\frac{\partial i(z,t)}{\partial z} = -G\, v(z,t) - C\frac{\partial v(z,t)}{\partial t} \tag{2.17}$$

Particularly, in the sinusoidal steady-state condition, the equations above can be simplified to yield

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.18}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.19}$$

Upon application of derivative in both terms of equations (2.16) and (2.17) the following second order differential equations are obtained:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.20}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{2.21}$$

where,

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.22}$$

is the propagation constant, which is dependent on frequency. Solving the differential equations above it is possible to obtain the following expressions for the current and voltage of the traveling waves in any specific point of the transmission line:

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.23}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \tag{2.24}$$

where the wave propagation in the +z and –z directions is given by the terms $e^{-\gamma z}$ and $e^{\gamma z}$ respectively. Applying the simplified equation obtained for the sinusoidal steady-state (2.18) on equation (2.23) the following expression for the current over the line will be give by

$$I(z) = (V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}) \frac{\gamma}{R + j\omega L} \tag{2.25}$$

Given that the obtained result must be equivalent to (2.24) we conclude that $I_0^+ = V_0^+ \frac{\gamma}{R+j\omega L}$ and $I_0^- = V_0^- \frac{\gamma}{R+j\omega L}$ and define the transmission line characteristic impedance, Z_0, as

$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{V_0^-}{I_0^-} = \frac{R + j\omega L}{\gamma} \tag{2.26}$$

If the line is terminated by a load Z_L at $z = 0$ (Fig. 2.8), assuming that the source of the wave is located at a position $z < 0$, the following condition must be verified

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_0^+ + V_0^-}{V_0^+ - V_0^-} Z_0 \tag{2.27}$$

where V_0^+ and $V_0^-$are the amplitude voltages of the incident and reflected waves respectively. The voltage reflection coefficient, Γ, which is the amplitude of the reflected wave normalized to the incident wave amplitude, can be derived from the previous equation

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.28}$$

To maximize the power transfer to the load, the reflection should be non-existent, i.e., $\Gamma = 0$, which, only occurs when $Z_L = Z_0$, according to (2.28), and then the load is matched to the line

characteristic impedance. Usually in RF the characteristic impedance of an antenna is 50 Ω, so the first block of a receiver must have the input impedance matched to the same value.

2.2.2 Scattering Parameters

Traditional system characterization used in low-frequencies trough open and short-circuit measurements is not possible at high frequencies, since the current and voltage measurements involve the magnitude and phase of the travelling wave [18]. Therefore, at high frequencies, since the device length is no longer negligible relatively to the wavelength of the travelling waves, network characterization must be done through different parameters. The scattering parameters, or S-parameters, relate the voltages of the incident and reflected waves, at n-ports, through the scattering matrix,

$$\begin{bmatrix} V_1^- \\ \vdots \\ V_n^- \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & & \vdots \\ S_{n1} & \cdots & S_{nn} \end{bmatrix} \begin{bmatrix} V_1^+ \\ \vdots \\ V_n^+ \end{bmatrix} \tag{2.29}$$

where V_i is the voltage amplitude on port i and the signal, + or -, relates to the incident and reflected wave, respectively. To determine a specific s-parameter, the following expression is used

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+ \neq 0, k \neq j} \tag{2.30}$$

This means that an s-parameter S_{ij} is determined as the ratio between the reflected wave voltage at port *I* and the incident wave at port *j*, when the other ports are terminated with a matched load so that reflections are avoided. These parameters can be measured directly using a network analyzer, which allows an accurate network characterization without the need to know every detail of the circuit inside the network.

In the specific case of a two-port network, the s-parameters can be designated according to their physical meaning as follows [13]:

- ✓ S_{11} – Input reflection coefficient
- ✓ S_{21} – Forward voltage gain
- ✓ S_{12} – Reverse voltage gain
- ✓ S_{22} – output reflection coefficient

Figure 2.9 – Schematic representation of a Two-Port Network with the incident and reflected waves.

The s-parameters are particular important in receiver front-ends, since they are helpful in LNA design, due to the need of input matching, and are also associated with the concept of return loss, which is a figure of merit for signal reflection, indicating the fraction of the incident power that is reflected back to the source. The input return loss is usually included in LNA's technical specifications and is defined as

$$RL = -20\,log(|s_{11}|) \tag{2.31}$$

Naturally, the aim is to minimize the reflected power, so that more power is transferred to the load. Usually, designers aim for at least 10 dB return loss, meaning that only a maximum of 10% of the total power is reflected back to the source.

2.3 Low Noise Amplifiers

The low noise amplifier (LNA) is an electronic amplifier used to amplify weak signals, that can be, regarding bandwidth, narrowband, multi-band or wideband [14-15]. It is typically used as the first stage of amplification. In order to maximize the power transfer, the LNA input impedance should be matched with the antenna's characteristic impedance. The LNA must provide enough gain for the desired SNR while simultaneously keeping a low noise factor to minimize the introduction of noise in the system. To accomplish the above requirements in a system consisting of several blocks connected in cascade, further considerations are needed. The overall noise factor of a cascade of stages is given by Friis equation [16] which can be written as:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{2.32}$$

where F_n and G_n are the noise factor and the available power gain of the n^{th} stage, respectively. From (2.32), it is clear that the noise factor of the first stage, *i.e.* of the LNA, is the dominant term and that if its gain is high enough it will significantly reduce the noise contribution of the subsequent stages.

The overall performance of stages in a cascade, regarding linearity, can be characterized by [1]:

$$\frac{1}{IIP_3} = \frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} + \frac{G_1 G_2}{IIP_{3,3}} + \cdots \quad (2.33)$$

with $IIP_{3,i}$ and G_i being the third-order intercept point (input referred) and the power gain of the i^{th} stage, respectively. The overall system linearity is limited by the performance of the stage with the worst IIP_3.

The IIP_3 of the last stage is directly related to the gain of the preceding stages, but at the same time a high gain for the first stage is necessary for a low noise figure. Therefore, there must be a compromise between noise and linearity.

2.3.1 Narrowband LNA's

- ***Common-source LNA with degeneration***

One of the most used topologies to design a narrowband LNA is the common-source (CS) LNA with inductive degeneration (Fig. 2.10) since this topology allows a low noise figure, high gain and easy input matching.

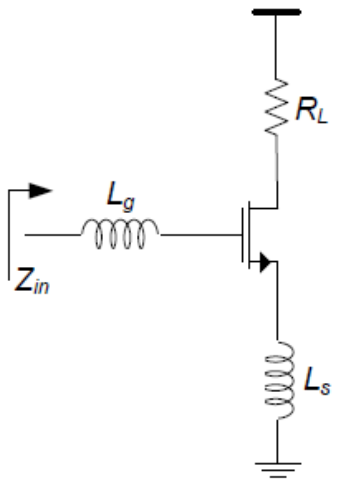

Figure 2.10 – Common-source LNA with inductive degeneration adopted from [10].

The input impedance of the CS LNA is given by

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \quad (2.34)$$

where the inductances, L_g and L_s, are chosen so that they resonate with the device capacitance C_{gs} at the frequency of operation which is expressed as

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \qquad (2.35)$$

This allows the elimination of the imaginary component of Z_{in} and matches the term $\frac{g_m}{C_{gs}} L_s$ to 50 Ω. Given that the gain of the device is proportional to g_m, the inductance L_g introduces some freedom in the design of the LNA. One of the advantages of this configuration is the improvement of the noise factor due to the use of inductors, which are ideally noiseless. However, their use increases significantly the die area of the LNA which, combined with RF options (thick metal layer for high Q inductors), lead to an increase of the production costs.

2.3.2 Wideband LNA's

- ***Common-source with resistive input matching***

Resistive input matching is one the simplest ways to obtain a stable input impedance. This technique, which is employed in the CS stage (Fig. 2.11), uses a resistor in parallel with the amplifier input.

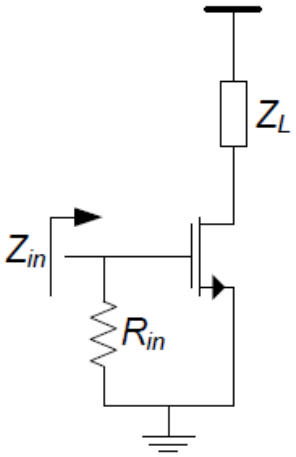

Figure 2.11 – Common-source stage with resistive input matching adopted from [10].

Unfortunately, the use of a resistor is associated with the introduction of a significant amount of noise.

Let us assume that the amplifier has an available power gain A_p and a noise power at output, P_n due to internal sources only. If the source has an impedance R_s, the noise factor can be computed using equation (2.37) and yields the following result

$$F = \frac{4k_B T R_S A_P + 4k_B T R_{in} A_P + P_n}{4k_B T R_S A_p} = 2 + \frac{P_n}{4k_B T R_s A_p} \qquad (2.36)$$

to which a noise figure of at least 3 dB ($NF \geq 3\ dB$) is associated.

- ***Common-gate***

One of the most widely used topologies in the implementation of LNA's is the common gate topology (Fig. 2.12). One of the reasons for this fact is that it has an intrinsic wideband response.

In a first order approximation, the input impedance is given by $\frac{1}{g_m}$, and g_m can be dimensioned easily in order to obtain the input impedance matching.

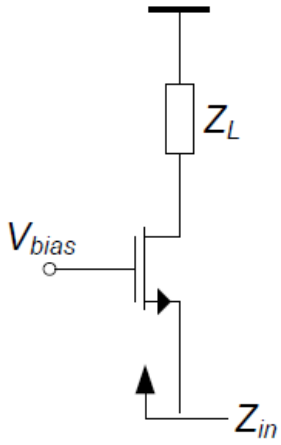

Figure 2.12 – Common-gate LNA adopted from [10].

The lower bound of the noise factor can be estimated considering only the transistor thermal noise level. If it is input referred, the noise factor can be written as

$$F = 1 + \gamma g_{d0} R_s = 1 + \frac{\gamma}{\alpha} g_m R_S \qquad (2.37)$$

defining α as $\frac{g_m}{g_{do}}$. As stated earlier, for long channel devices the noise excess factor, γ, is $\frac{2}{3}$ and short-channel effects can be neglected ($\alpha = 1$) [21] with matching $g_m R_S = 1$. The minimum noise factor can then be estimated to be approximately $F = \frac{5}{3}$, which corresponds to $NF \approx 2.2\ dB$. However, since g_m is imposed by the matching condition, the gain is only dependent on the load Z_L and, while increasing Z_L causes an increase in gain, it will also generate increased levels of noise. The possible gain being, therefore, limited.

In practice, the noise figures for a CG-LNA are above 3 dB.

- ***LNA with resistive shunt feedback***

In Fig. 2.13 (a), it is shown a wideband LNA using the feedback resistor R_S for matching. According to the incremental model depicted in Fig. 2.13 (b) the input impedance can be expressed as

$$Z_{in} = \frac{R_F + Z_L}{sC_{gs}(R_F + Z_L) + 1 + g_m Z_L} = \left(\frac{1}{sC_{gs}} // \frac{R_F + Z_L}{1 + g_m Z_L} \right) \qquad (2.38)$$

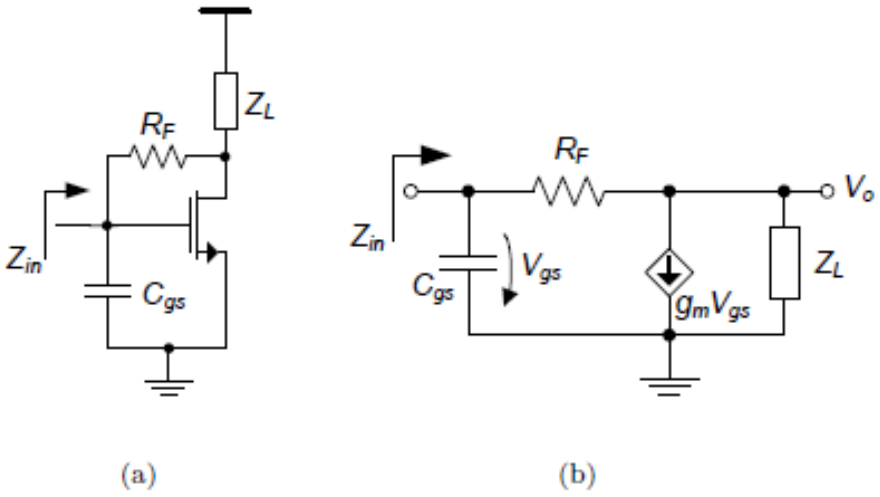

Figure 2.13 – LNA with resistive shunt feedback: (a) schematic representation; (b) small signal model (low and medium frequencies) adopted from [9].

Given that the previous equation is dependent on many variables, some assumptions need to be made in order to obtain a more simplified expression. For frequencies such that C_{gs} becomes negligible, the gate can be seen as a high impedance and, assuming that $Z_L \gg R_F$, the input

impedance can be simply written as $\frac{1}{g_m}$. Analogously, using similar reasoning for the low frequency case, the gain is then written as

$$A_v = \frac{(1 - g_m R_F) Z_L}{R_F + Z_L} \qquad (2.39)$$

and if the load Z_L is high then $g_m R_F \gg 1$ and the gain is the simplified into

$$A_v \approx -g_m R_F \qquad (2.40)$$

This approximation is very useful regarding the noise factor [17], which can be expressed as

$$F = 1 + \frac{R_F}{R_S}\left(\frac{1 + g_m R_S}{1 - g_m R_F}\right)^2 + \frac{1}{R_s Z_L}\left(\frac{R_F + R_S}{1 - g_m R_F}\right)^2 + \frac{\gamma g_m}{\alpha R_s}\left(\frac{R_F + R_S}{1 - g_m R_F}\right)^2 \qquad (2.41)$$

Analyzing the equation above, it is clear that increasing the term $g_m R_F$ the noise factor is reduced and the gain enhanced, as expected. g_m is set by the matching condition, so R_F is the parameter available that can be increased. In this situation, the previous assumption to have a high load Z_L comparatively to R_F is no longer valid. Hence, in order to achieve optimal performance, R_F and g_m need to be carefully dimensioned.

2.3.3 Final remarks

In the previous sections, basic LNA architectures were presented in the single-ended form. However, a differential structure may be used instead. In order to perform the transformation from the antenna into a differential signal, a balun would be required, which would introduce extra losses and additional noise in the system.

As we know the narrowband LNAs present good noise figure, high gain, and accurate matching due to the LC tuning for the frequency of interest, but inductors occupy a large area and increase significantly the cost of the chip.

The wideband LNAs are typically inductorless, suitable for systems with low area and with non-critical specifications. With the scaling of CMOS technology it is possible to achieve low power, low cost, and an acceptable noise figure, and inductorless wideband LNAs became a competitive choice to implement multi-band LNAs. These can be implemented by using narrowband LNAs in a multiple input stage, or by wideband LNA with a band-pass filter for each band.

Narrowband LNA:

- ✓ Good noise figure
- ✓ High gain
- ✓ Accurate matching due to the LC tuning for the frequency of interest
- ✓ Large area associated to the inductors
- ✓ Significant increase in chip cost

Wideband LNA:

- ✓ Suitable for systems with low area and non-critical specifications

Due to scaling of CMOS technology it is possible to achieve:

- ✓ Low power
- ✓ Low cost
- ✓ Acceptable noise figure

Chapter 3

3 Noise and Nonlinear distortion in LNAs

3.1 Noise

Noise, in electronics, manifests as a random fluctuation in an electrical signal and is characteristic of all electronic circuits. It manifests itself as a random variable that can be introduced by physical phenomena related with the nature of the materials or by external interferences. Noise has a non-deterministic nature and its instantaneous value is not predictable being, therefore, impossible to eliminate *a priori*.

Given that noise is present in every electronic circuit, it is important to analyze it carefully and then we need to develop methods to help minimize its effects.

In the following section, the main sources of noise present in CMOS transistors are presented and described [14-4].

3.1.1 Thermal Noise

Thermal noise, also known as Johnson-Nyquist noise, is the electronic noise generated by the thermal agitation of the charge carriers (typically electrons) inside an electrical conductor at equilibrium causing a variation in current, which is present regardless of the applied voltage. The thermal noise power is proportional to the temperature (absolute) and can be quantified by:

$$P = k_B T \Delta f \tag{3.1}$$

where k_B is Boltzmann's constant and Δf represents the bandwidth of the system.

The average noise power generated in a resistor is given by

$$\overline{\overline{V_{th}^2}} = 4k_B T R \Delta f \tag{3.2}$$

and can be modeled using an ideal resistor (noise free) in series with a voltage source or in parallel with a current source, both of which are responsible for the introduction of noise in the model (Fig. 3.1).

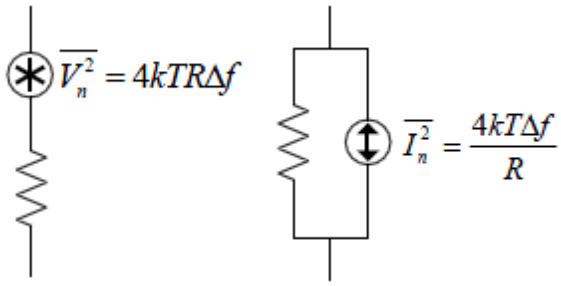

Figure 3.1 – Models for thermal noise in a resistor adopted from [9].

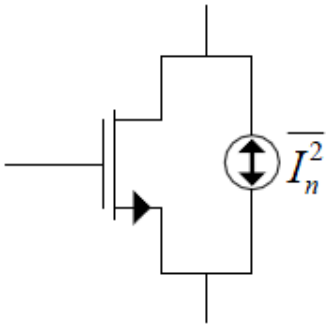

Figure 3.2 – Model for thermal noise in a MOSFET adopted from [10].

In the case of MOS transistors, carrier motion through the channel is also a source of thermal noise which can be represented by a current source in parallel with the conducting channel (Fig. 3.2).

If the transistor is operating in the triode region, the noise generated in the channel is given by [19]:

$$\overline{I_n^2} = 4k_B T\gamma g_{d0}\Delta f \tag{3.3}$$

where g_{d0} is the channel conductance at zero drain-source voltage and γ is the noise excess factor (NEF) which is equal to 1 for this bias condition ($V_{DS} = 0$). This result can be extended to long-channel MOSFET devices operating in saturation [20]:

$$\overline{I_n^2} = 4k_B T\gamma g_m\Delta f \tag{3.4}$$

with $\gamma = 2/3$, while for short-channel and submicron MOSFET's γ takes higher values [21].

3.1.2 Flicker Noise

Flicker noise is also often referred to as $1/f$ noise or pink noise (even though both terms have wider definitions) due to its $1/f$ or pink power density spectrum.

In FET's, it originates in a somewhat unpredictable physical phenomenon which is related with the interface between the gate oxide and the silicon substrate (SiO_2/Si). This type of noise is associated with fluctuations in the number of carriers in the channel due to trapping and release of the carriers in the SiO_2/Si. Due to its $1/f$ dependence, flicker noise becomes dominant at low frequencies. An adequate model for its representation consists of a voltage source in series with the gate, expressed as

$$\overline{V_{nf}^2} = \frac{k_f}{c_{ox} W L f^{a_f}} \tag{3.5}$$

with k_f being a process dependent and bias independent constant, c_{ox} being the gate oxide capacitance per unit area and W and L the width and length of the MOSFET respectively. The values of k_f vary depending on the quality of the fabrication process, being lower for cleaner fabrication processes. k_f is also lower in p-channel devices, when comparing the value to the one for n-channel devices, flicker noise being therefore more relevant in the latter case. The exponent a_f is close to 1 but can vary between 0.7 and 1.2 [20]. This type of noise is still under study regarding its origin and modeling.

3.1.3 Noise Figure

The noise figure (NF) and the noise factor (F) are measures of the degradation of the signal-to noise ratio (SNR) and serve as a number by which the performance of a radio receiver can be specified.

Considering a circuit characterized by a 2-port network, the noise factor is defined as the ratio between the total noise power at the 2-port output and the 2-port output noise power due to the input noise sources only and is given by:

$$F = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ the\ source} \tag{3.6}$$

The noise figure is simply the noise factor expressed in decibels (dB), i.e. NF can be expressed as

$$NF = 10\,log\,F \tag{3.7}$$

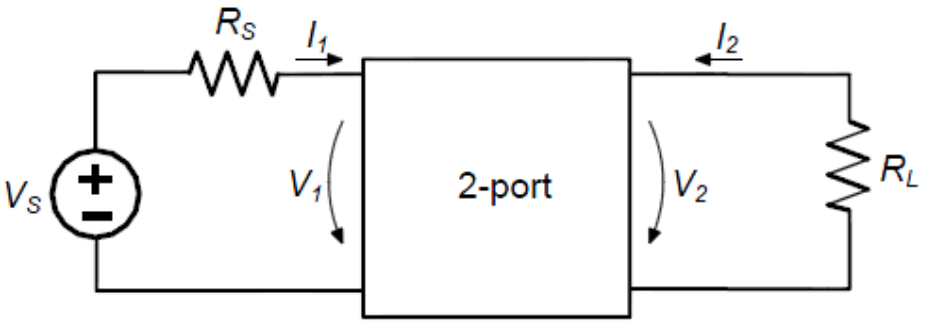

Figure 3.3 – Noisy 2-port network with gain A adopted from [10].

As an example, let us consider a noisy 2-port network represented in Fig. 3.3. The noise factor is given by

$$F = \frac{N_2}{A^2 N_1} \tag{3.8}$$

with N_1 and N_2 being the noise power available at the 2-port input and output, respectively.

If the ports are adapted and a power signal S_1 is applied from the generator, then according to the power transfer theorem, the signal must be completely transferred to the 2-port and so is the signal power signal S_2 from the 2-port output to the load resistor R_L. The power gain is then given by

$$A^2 = \frac{S_2}{S_1}. \tag{3.9}$$

Replacing in eq. (3.8), the noise factor can then be written as

$$F = \frac{\frac{S_1}{N_1}}{\frac{S_2}{N_2}} = \frac{(S/N)_i}{(S/N)_o}. \tag{3.10}$$

The previous equation relates the noise factor with the SNR's at the input and output of the 2-port, showing the degradation of the SNR caused by the 2-port. If no additional noise is introduced by the 2-port the value of F should be unity ($F = 1$).

3.2 Nonlinear Distortion

Nonlinear distortion is a term used to describe the phenomenon of non-linearity between the input and output of a system. The performance, regarding linearity, is characterized by the 1dB

compression point and the 3rd-order intermodulation product, both of these parameters appearing in the systems' specifications.

A linear system generates an output signal proportional to the input signal. However, for many devices, a linear model is only applicable for small signals. Most devices have non-linear characteristic, and if they are memoryless and time invariant, the input-output relationship may be represented by a polynomial or Taylor series, *i.e.*

$$y = \sum_{i=0}^{n} a_i x^i = a_0 + a_1 x + \cdots + a_n x^n \tag{3.11}$$

The type of non-linearity is directly related to the terms used in the description of these devices, its representation being more accurate if more terms are used.

3.2.1 Harmonics

Nonlinear devices generate harmonics. Characterizing a nonlinear device by a 3rd-order polynomial is typically a good approximation and it allows simplification to be done in the calculations. Let us assume sinusoidal input signal given by

$$v_i(t) = V_m \cos(\omega_f t)\,. \tag{3.12}$$

Therefore the output will be expressed as

$$y(t) = a_0 + a_1 V_m \cos(\omega_f t) + a_2 V_m^2 \cos^2(\omega_f t) + a_3 V_m^3 \cos^3(\omega_f t) \tag{3.13}$$

Taking into account the trigonometric relations $cos^2 x = \frac{1+cos\,2x}{2}$ and $cos^3 x = \frac{3\cos x + cos\,3x}{4}$, equation (3.14) can be rewritten as

$$y(t) = \underbrace{a_0 + \frac{a_2 V_m^2}{2}}_{DC\ component} + \underbrace{\left(a_1 V_m + \frac{3a_3 V_m^3}{4}\right)\cos(\omega_f t)}_{1^{st} Harmonic\ (fundamental)} + \underbrace{\frac{a_2 V_m^2}{2}\cos(\omega_f t)}_{2^{nd}\ Harmonic} + \underbrace{\frac{a_3 V_m^3}{4}\cos(\omega_f t)}_{3^{rd} Harmonic} \tag{3.14}$$

An n-order nonlinearity will generate n harmonics, each with a frequency that is multiple of the fundamental frequency, ω_f.

3.2.2 Intermodulation product

Let us assume that instead of applying a single sinusoidal signal at the non-linear input, two signals with different frequencies, ω_1 and ω_2, are now applied. The input signal can then be written as

$$v_i(t) = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t) \tag{3.15}$$

Intermodulation between both frequencies will generate additional signals that are not simply harmonic frequencies (multiples of each frequency), but also sum and difference frequencies of the input signal frequencies and multiples of those sum and difference frequencies, *i.e.* Intermodulation products appear at frequencies $n\omega_1 \pm m\omega_2$.

For the considered input, given by equation (3.15), the Intermodulation products generated at the output are given by

$$\begin{aligned}
&y(t) \\
&= a_0 + a_1(V_1 \cos(\omega_1 t)\, V_2 \cos(\omega_2 t)) \\
&+ a_2 \left[\begin{array}{l} \frac{V_1^2}{2}(1 + \cos(2\omega_1 t)) + \frac{V_2^2}{2}(1 + \cos(2\omega_2 t)) + \\ V_1 V_2(\cos\big((\omega_1 + \omega_2)t\big) + \cos\big((\omega_1 - \omega_2)t\big)) \end{array}\right] \\
&+ a_3 \left[\begin{array}{l} \left(\frac{3}{4}V_1^3 + \frac{3}{2}V_1 V_2^2\right)\cos(\omega_1 t) + \left(\frac{3}{4}V_2^3 + \frac{3}{2}V_2 V_1^2\right)\cos(\omega_2 t) + \\ \quad \frac{3}{4}V_1^2 V_2\big(\cos\big((2\omega_1 + \omega_2)t\big) + \cos\big((2\omega_1 - \omega_2)t\big)\big) + \\ \quad \frac{3}{4}V_2^2 V_1\big(\cos\big((2\omega_2 + \omega_1)t\big) + \cos\big((2\omega_2 - \omega_1)t\big)\big) + \\ \qquad \frac{3}{4}V_1^3 \cos(3\omega_1 t) + \frac{3}{4}V_2^3 \cos(3\omega_2 t) \end{array}\right]
\end{aligned} \tag{3.16}$$

The appearance of the different frequencies is illustrated in Fig. 3.4 for the particular case of a device with non-linearity of 3rd order.

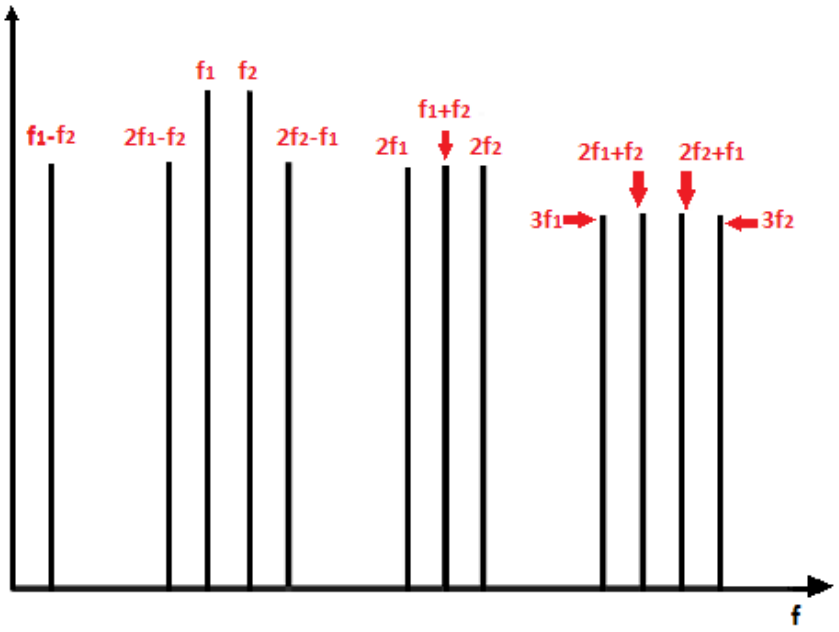

Figure 3.4 – Frequency spectrum showing the Intermodulation products of a 3rd order nonlinear device.

3.2.3 1 dB Compression Point

The 1 dB compression point is a linearity measure of a circuit and it specifies the output signal power that is lower than the nominal output of the ideal (linear) circuit by 1 dB (Fig. 3.5).

Past this point, the saturation is reached and consequently degrades the signal. A linear system is out of its normal operation mode if it is operating above P_{1dB}.

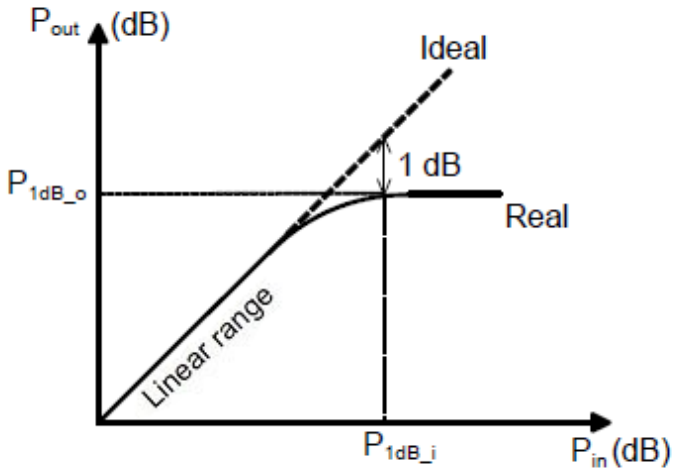

Figure 3.5 – Definition of the 1 dB compression point.

3.2.4 Third-order intercept point

The third-order intercept point (IP3) is defined as the interception between the curves of the power output of the fundamental frequency and the third-order intermodulation product (IM3) if both these curves were linear, *i.e.* when the amplitude for both is the same. In order to determine the intercept point, a practical rule consists in using the position of the 1 dB compression point as a starting point, since the 1 dB compression point should fall 10dB below the intercept point. The specification of the IP3 is usually input-referred (*IIP3*), but it can also be output-referred (*OIP3*). An example of the latter is illustrated in Fig. 3.6.

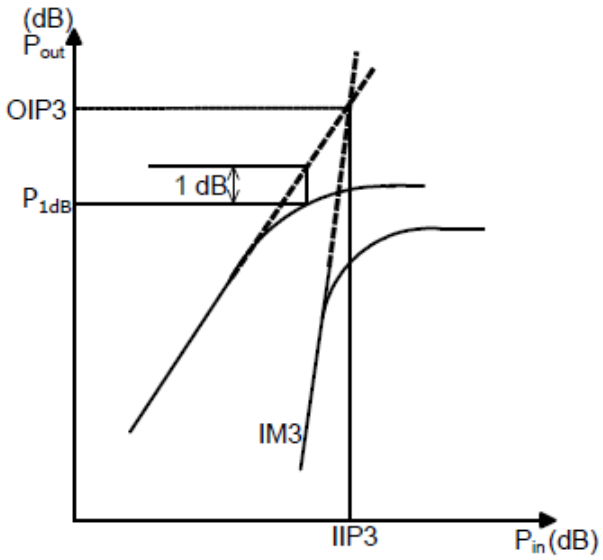

Figure 3.6 – Definition of IP3 adopted from [10].

Chapter 4

4 Common Gate and Common Source Stages

4.1 Common-Source Stage

Common-Source amplifier (Fig. 4.1) is one of the basic single-stage amplifiers, typically used as transconductance impedance or a voltage. This stage has the main objective high input and output impedances and high voltage gain. Note that this stage is not good for a single stage wideband LNA [21].

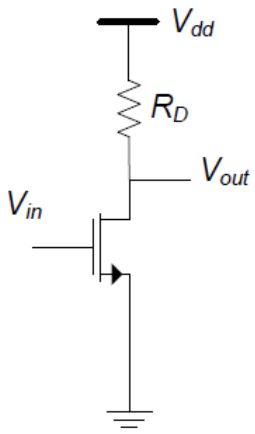

Figure 4.1 - Common-Source amplifier

Now, by analyzing the small-signal model, equations are going to be derived for the gain in two different ways. First we are going to start with the simplest transistor model, where we neglected r_0 and finally we are going to derive a more complex model, considering the r_0.

4.1.1 Low frequency model neglecting r_0

In this stage, the input signal is going to be injected to the gate, which is isolated from the transistor channel, thus for low frequencies the input impedance is considered infinite. Note that the bulk and the source are connected to the ground, which means that there is no body effect.

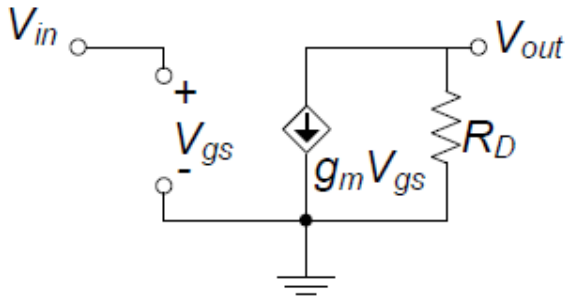

Figure 4.2- Small-signal model of Common-Source amplifier neglecting r_0

Gain

By analyzing the small-signal model shown in Fig. 4.2 we obtain

$$V_{out} = -g_m . V_{in} . R_D \qquad (4.1)$$

$$\Leftrightarrow \qquad \frac{V_{out}}{V_{in}} = -g_m . R_D \qquad (4.2)$$

$$\Leftrightarrow \qquad A_{vCS} = -g_m . R_D \qquad (4.3)$$

4.1.2 Low frequency model with r_0

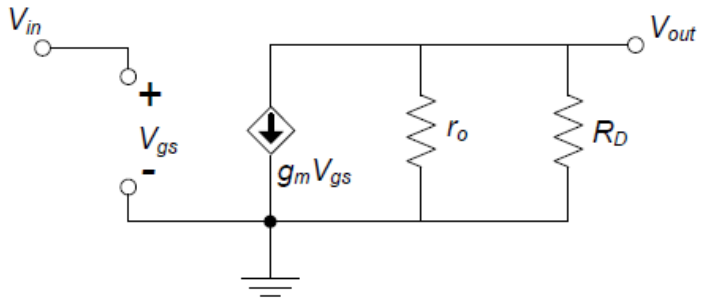

Figure 4.3- Small-signal model of Common-Source amplifier with r_0

Gain

By analyzing the circuit on Fig. 4.3 we can see that r_0 is in parallel with the load resistor, R_D, and therefore, the gain is given by

$$A_{vCS} = -g_m . \frac{r_0 . R_D}{r_0 + R_D} . \qquad (4.4)$$

4.2 Common-Gate Stage

The common gate stage (Fig. 4.4) is a known amplifier topology that will be used as one of the stages in the proposed LNA. A theoretical analysis will be shown to obtain the key parameters (input matching, gain and noise) and two types of approximation are performed.

Now, we are going to review some expressions for input impedance, gain, and noise. For each parameter will be derived two equations, one for the each model chosen to represent the transistor.

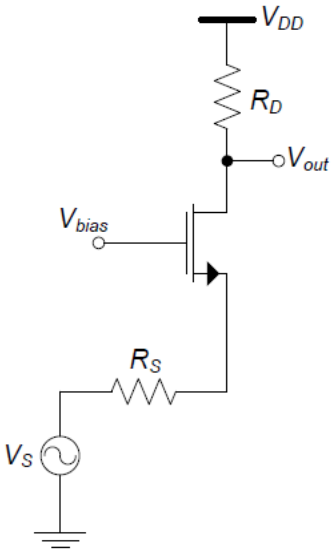

Figure 4.4- Common Gate stage

4.2.1 Low frequency model neglecting r_0

In Fig. 4.5 is represented the common gate stage small signal model for low frequencies. For simplify, the output impedance of the transistor is neglected. As the signal, V_{in}, is applied in transistor's source terminal, we have to consider the body effect, represented in the model by a voltage controlled current source which depends on source-bulk voltage, V_{sb}.

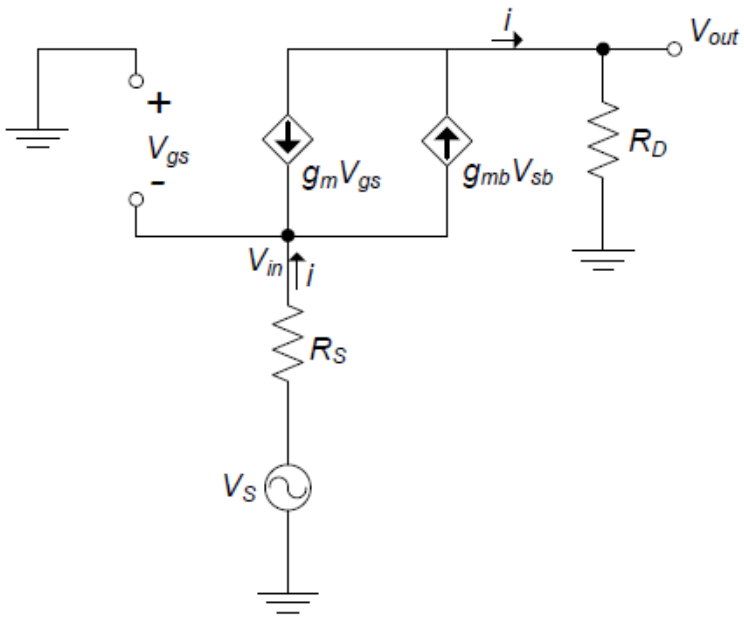

Figure 4.5- Common Gate stage small signal model for low frequencies

Gain

Using the small-signals analyses it is possible to obtain the gain. At output, the signal is given by

$$V_{out} = R_D.i\,. \qquad (4.5)$$

For this case $V_{sb} = -V_{gs} = V_{in}$, and the expression in order to express the current i is

$$i = g_{mb}.V_{sb} - g_m.V_{gs} \qquad (4.6)$$

$$\Leftrightarrow \qquad i = V_{in}.(g_m + g_{mb}) \qquad (4.7)$$

After this, we can obtain the CG gain, substituting on (4.5)

$$A_{vCG} = \frac{V_{out}}{V_{in}} = R_D.(g_m + g_{mb}). \qquad (4.8)$$

Input Impedance

Using the scheme of Fig. 4.6, it was possible to show the expression for the input impedance, which is viewed from the source.

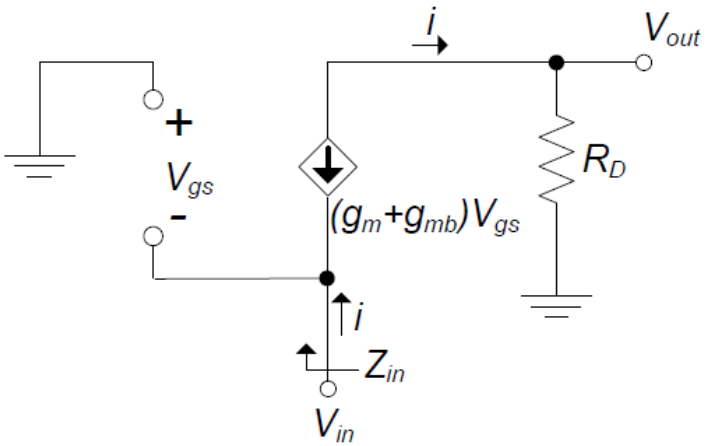

Figure 4.6- Input impedance

By analyzing the circuit above, we can see that the expression of current i is given by

$$i = -V_{gs}.(g_m - g_{mb}) \qquad (4.9)$$

$$\Leftrightarrow$$

$$i = V_{in}.(g_m + g_{mb}) \qquad (4.10)$$

and the input impedance is given by

$$Z_{incG} = \frac{1}{g_m + g_{mb}} \qquad (4.11)$$

4.2.2 Low frequency model with r_0

In previous section (4.2.1.), in order to simplify, it was considered that r_0 (transistor output impedance) was infinite. Now, in this section we are going to derive the same expressions, but considering the value of r_0.

In Fig. 4.7 we can see the r_0 is modeled with a resistor between the source and the drain of the transistor.

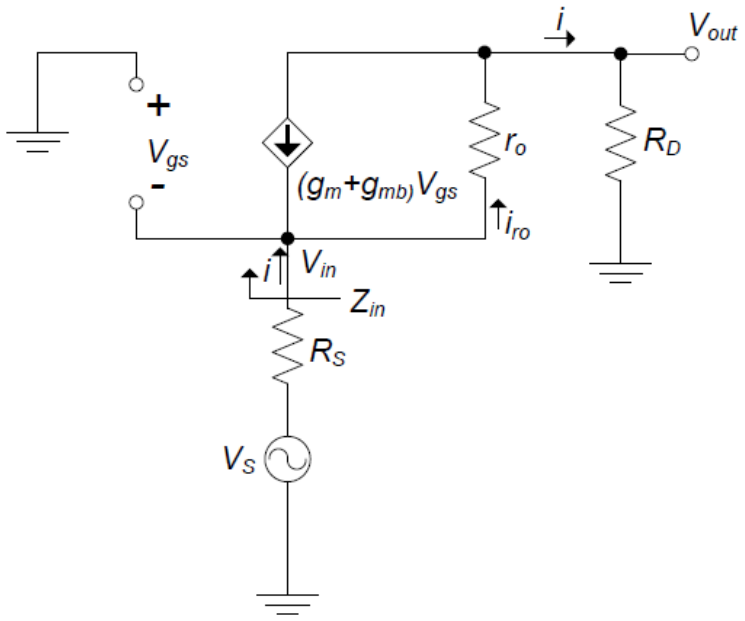

Figure 4.7- Small-signal model of Common-Gate stage with r_0

Gain

Analyzing the small-signals, it is possible to obtain the gain. We can see that the current flowing in R_S is the same that goes for R_D, so

$$V_{out} = R_D . i \qquad (4.12)$$

$$\Leftrightarrow$$

$$\frac{V_{out}}{R_D} = i \qquad (4.13)$$

and the current i_{r0} is given by

$$i_{r0} = \frac{V_{out}}{R_D} + V_{gs} . (g_m + g_{mb}). \qquad (4.14)$$

As we know,

$$V_{gs} = R_S . i - V_S \qquad (4.15)$$

And replacing (4.13), we obtain

$$V_{gs} = R_S . \frac{V_{out}}{R_D} - V_S \qquad (4.16)$$

In terms of Kirchhoff's Voltage Law (KVL), we can expressed the output voltage (V_{out}) as,

$$V_{out} = V_S - R_S . i - r_0 . i_{r0} \qquad (4.17)$$

$$\Leftrightarrow$$

$$\frac{V_{out}}{V_S} = \frac{R_D . (1 + r_0 . (g_m + g_{mb}))}{R_D + r_0 + R_S . (1 + r_0 . (g_m + g_{mb}))} = A_v \ . \qquad (4.18)$$

Finally, assuming $R_S = 0$, the gain of CG stage is given by

$$A_{vCG} = \frac{R_D . (1 + r_0 . (g_m + g_{mb}))}{R_D + r_0} \qquad (4.19)$$

Input Impedance

Analyzing Fig. 4.6, the input voltage is given by the sum of drop voltages in r_0 and R_D, in other words,

$$V_{in} = r_0 . i_{r0} + R_D . i \qquad (4.20)$$

and as we know,

$$i_{r0} = i + V_{gs} . (g_m + g_{mb}) \qquad (4.21)$$

Now, we can replace (3.21) on (3.20), where $V_{gs} = -V_{in}$ and the input impedance is given by

$$Z_{inCG} = \frac{v_{in}}{i} \qquad (4.22)$$

$$\Leftrightarrow$$

$$Z_{inCG} = \frac{r_0 + R_D}{r_0 . (g_m + g_{mb}) + 1} \qquad (4.23)$$

Chapter 5

5 Balun LNA with Noise Cancellation

5.1 Wideband Balun-LNA with Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling

In a receiver path, since typically, the antenna and RF filters are single-ended, it is very important to have a LNA with single-ended configuration input. A differential signal in the receiver is preferred to reduce harmonic distortion and to reject power supply and substrate noise [23]. Traditionally, we have an external balun that converts single-ended signals to differential, but it introduces losses and degrades the receiver NF. A balun LNA is a very good solution to convert a single-ended to a differential signal, which simplifies the design avoiding the external balun [23].

A balun LNA, in which the thermal noise of CG-transistor is canceled because this noise appears in phase at two outputs and their gains are in opposition, is proposed in [23]. The gain is doubled and the noise is reduced when the output signals are balanced. It can also be shown that the distortion introduced by M_1 is also cancelled.

The differential LNA is represented in the Fig. 5.1, where its operation principle is illustrated. The output signal's CG stage and the input signal have the same sign while the output signal's CS stage is in opposition. The thermal noise produced by the transistor M_1, represented by the current source I_{n1}, originates a noise voltage at the input $V_{n,in}$ since it flows into Rs. At the CG output $V_{n,out1}$ the noise voltage appears with opposite phase while at the CS output $V_{n,out2}$ it appears with the same phase. Consequently, the CG thermal noise is canceled. Note that the gain of the two stages has to be the same to full noise cancelation.

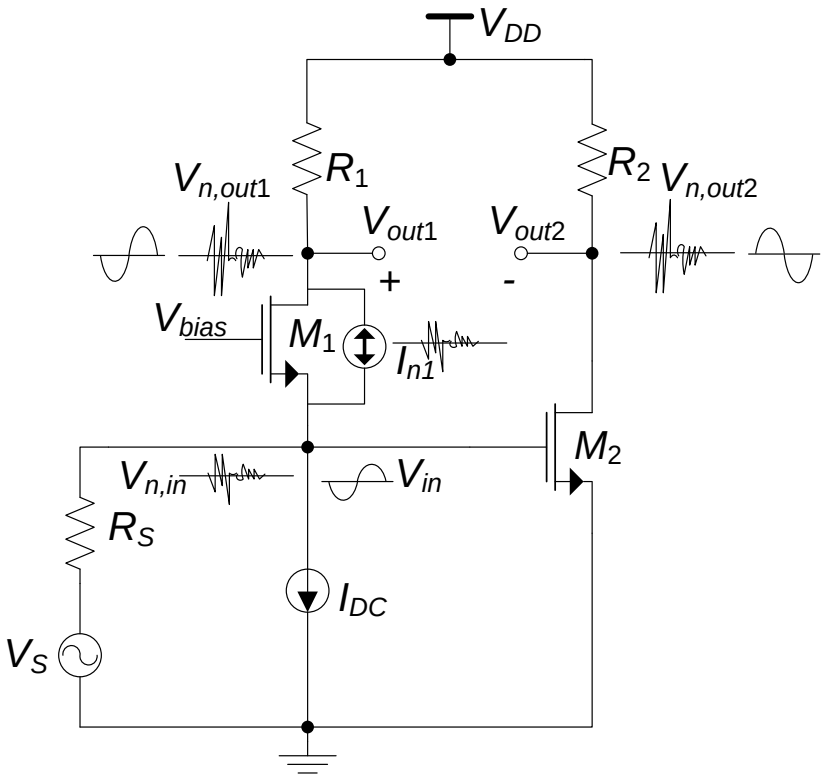

Figure 5.1- Balun LNA with noise canceling of CG-transistor adopted from [23]

5.1.1 Input Impedance

The LNA input impedance is given by the parallel of the CG and CS stages, in other words,

$$Z_{in} = (Z_{incG} // Z_{incS})\,. \qquad (5.1)$$

If it is assumed that the CS input impedance is very high,

$$Z_{in} = Z_{in\_CG} = \frac{sC_L r_{o1} R_1 + r_{o1} + R_1}{as^2 + bs + c} \qquad (5.2)$$

where $a = C_S C_L r_{o1} R_1$, $b = C_S(r_{o1} + R_1) + C_L R_1(r_{o1}(g_{m1} + g_{mb1}) + 1)$ and $c = r_{o1}(g_{m1} + g_{mb1}) + 1$.

For the low frequency approximation, the input impedance can be given by

$$Z_{in} = Z_{incG} = \frac{r_{o1} + R_1}{r_{o1}(g_{m1} + g_{mb1}) + 1}\,. \qquad (5.3)$$

5.1.2 Gain

The differential voltage gain of the LNA is obtained from the difference of the common-gate (CG) stage and the common-source (CS) stage gains [24].

$$A_v|_{Diff} = \frac{R_1(r_{o1}(g_{m1}+g_{mb1})+1)}{sC_L r_{o1}R_1 + r_{01} + R_1} - \frac{(sc_{gd2} - g_{m2})r_{o2}R_2}{sr_{o2}R_2(c_{db2}+c_{gd2}) + r_{o2} + R_2}. \quad (5.4)$$

We can use the low frequencies approximation (4.19) and (5.4), which results:

$$A_v|_{Diff} = \frac{R_1(r_{o1}(g_{m1}+g_{mb1})+1)}{r_{01} + R_1} + g_{m2}\frac{r_{o2}R_2}{r_{o2}+R_2}\ , \quad (5.5)$$

to achieve noise cancelation and balun operation, which means converting a single-ended input to a differential output, the CG and CS stages have to be equal. Assuming $r_{o1}(g_{m1}+g_{mb1}) \gg 1$ for the same current and length of M_1 and M_2, $r_{o1} \approx r_{o2} \approx r_o$, and considering $g_{m1}+g_{mb1} = g_{m2} = g_m$ and $R_1 = R_2 = R_D$, we obtain,

$$A_v|_{Diff} = \frac{2r_o R_D g_m}{r_o + R_D}. \quad (5.6)$$

5.1.3 Noise factor

The noise factor at LNA output is going to be given by the sum of the noise power at CG and CS output stages, in which at the CG output, the noise power is originated by M_1 and R_1 and at the CS output the output the noise power is generated by M_2 and R_2. Additionally, the contributions of the noise by the CG stage is going to appear at the CS output, so as the noise contributions by the CS stage will appear at the CG stage. Under this condition it can be assumed an approximation for the expression of the noise factor of this circuit given by,

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} \quad (5.7)$$

5.1.4 Circuit Implementation

This LNA was designed for 50 Ω input impedance through of the equation (4.11) as a first approximation, fixing the transconductance of M_1 (biased with 2 mA). The R_1 e R_2 resistors have the value 200 Ω to provide a DC output level which avoids signal limitation and still provides enough voltage headroom to keep the transistors M_1 e M_2 in saturation. Thus, g_{m1} is adjusted in order to complete the matching requirements by increasing the transistor width (W_1) through the equation (5.3), while the length (L) is going to the minimum value allowed by the technology. The V_{bias}, DC voltage, is used to get adjust the DC current of M_2 to the same value of M_1. After this, g_{m2} is chosen in order to the gain of the two stages have the same value.

This design already produces some noise cancelation and provides enough gain for the LNA, but there is not too much freedom to maximize the gain. On the other hand, the noise factor might be reduced more effectively increasing the transconductance (g_m) than the load resistor R_D [23]. As the thermal noise of M_1 is canceled and its g_m have to be fixed to maintain the input matching, an alternative design procedure is to increase the transconductance of transistor M_2 and reduce the value of the resistor R_2 in the same proportion in order to maintain the gain.

5.2 MOSFET-Only Wideband Balun Low Noise Amplifier

In the MOSFET-Only low noise Amplifier the load resistors are replaced by PMOS transistors (Fig. 5.2), M_3 e M_4, operating in the triode region, what means these transistors behave, approximately, as linear resistors [7]. These transistors are modeled ideally by a resistor between the drain and source, $r_{ds} = \frac{1}{g_{ds}}$ where g_{ds} is the channel conductance.

After the resistors being replaced by MOSFETs, it was possible to optimize the initial circuit.

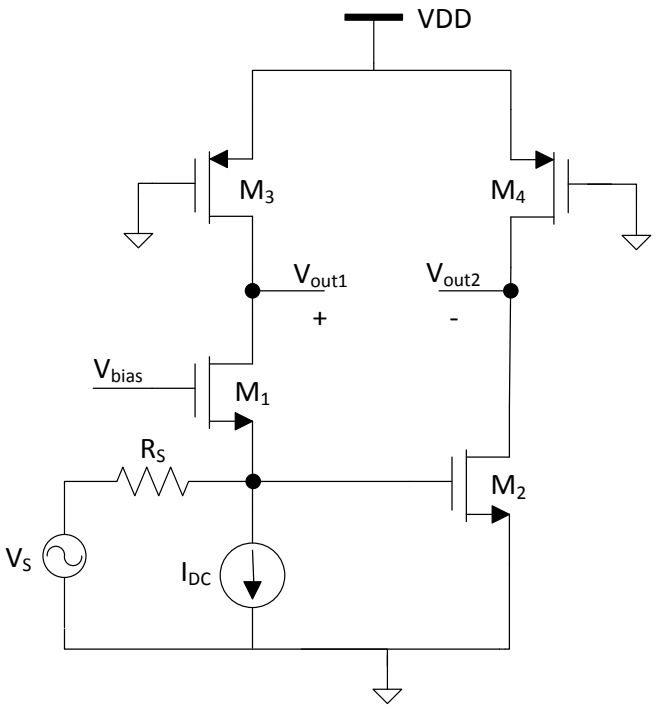

Figure 5.2- MOSFET - Only LNA

A MOS transistor is in the saturation region when its g_m is about the same value as g_{ds}. The MOS transistor operating in the triode region might be modeled by a resistor if $\frac{g_{ds}}{g_m} > 10$, otherwise the transistor had better be modeled by a resistor in parallel with a current source. Note that the equations for the gain, noise and input impedance of this circuit are the same of previous section.

5.3 A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications

Software-defined and reconfigurable multi-standard radio receivers have been drawing attention and are regarded for future radios, requiring multiple narrowband low noise amplifiers (LNA's) or a wideband LNA that can cover multiple frequency bands, the latter being the preferred option due to power saving and smaller complexity. This LNA should exhibit high gain, low noise figure (NF) and good impedance matching.

Traditional LNA's with on-chip inductors occupy large areas which counters the benefits associated with scaled digital CMOS. Several wideband inductorless LNA's have been proposed and can be divided into two categories:

- ✓ Common-source (CS) amplifier with resistive or active feedback
- ✓ Common-gate (CG) amplifier with g_m boosting or noise cancelling

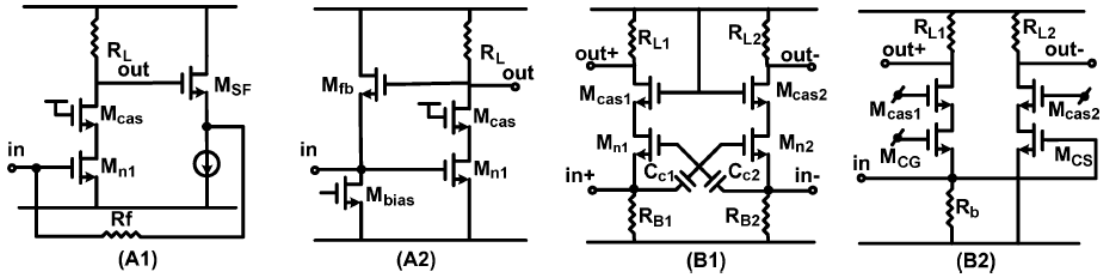

Figure 5.3- Previously proposed inductorless LNA's: (A1) CS LNA with resistive feedback; (A2) CS LNA with active feedback; (B1) CG LNA with g_m boosting; (B2) CG-CS LNA with noise cancelling adopted from [25].

In the first topology (Fig. 6.3 A1 and A2), impedance matching is achieved by the global resistive or active feedback which is defined as the feedback between the LNA output and input nodes. Unfortunately, at high frequencies the impedance matching degrades due to roll-off since the feedback signal is taken from the output node, which has relatively high gain and low bandwidth. Simultaneously, the nonlinear feedback transistor M_{fb} or the source follower transistor M_{SF} severely degrade linearity of the LNA due to the large swing of the output.

A CG LNA with g_m boosting is presented in Fig. 6.3 (B1). In this case, the power and NF are improved by a factor of 2 but the voltage gain ($A_v = 2g_m\, R_L = R_L/R_S$) is restricted by the impedance matching condition ($R_S = 1/2g_m$). The CG-CS LNA combined with noise canceling (Fig. 6.3 (B2)) exhibits good input impedance matching and low NF. While balanced output and noise canceling is simultaneously achieved under the condition $g_{mCG}\, R_{L1} = g_{mCS}\, R_{L2}$, this topology suffers from critical tradeoff between NF and supply voltage.

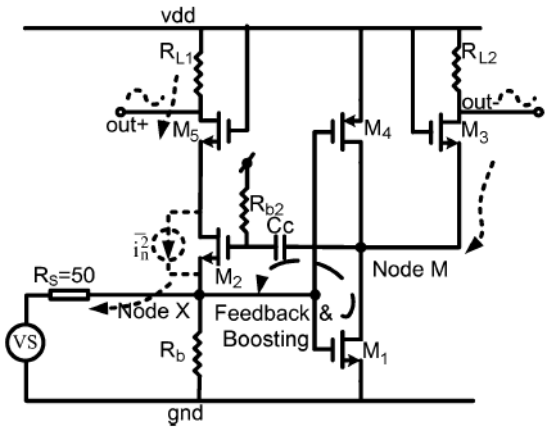

Figure 5.4 – Simplified schematic of the proposed LNA adopted from [25].

In order to lessen the conflicts between supply voltage, power and NF in the previous inductorless LNA configurations, a local negative feedback is introduced between the CG and CS stages (Fig. 5.4). The proposed LNA uses noise cancelation to eliminate the noise from the CG

transistor (M_2) and cascade transistor (M_3). The channel noise of M_2 undergoes subtraction at output nodes (Out+ and Out-) due to the two correlated and out-of-phase noise voltages at V_{out+} and V_x.

The local feedback is employed to allow low-voltage and low-power applications. In the CG stage, the g_m of M_2 is boosted by a factor of $1 + A_{VM}$ due to the negative feedback, while in the CS stage, the current steering leads to better gain and NF and diminishes the voltage drop on R_{L2}.

By distributing the power consumption among all components, depending on their noise contribution, NF optimization is achieved. In this design, the current steering in the CS stage and the interaction between the CG and CS stages introduces by the local feedback provide the opportunity to distribute the power consumption and voltage drop among resistors and transistors in order to achieve optimization. The relationship between A_{VM} and NF is briefly described in Fig. 5.5.

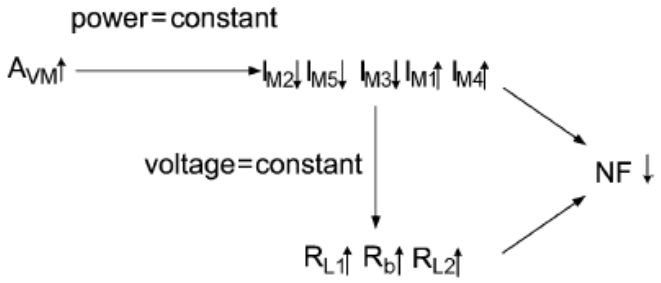

Figure 5.5- Schematic representation of the relationship between A_{VM} and NF adopted from [25].

Improvement of the linearity is attained by resorting to two kinds of distortion cancelling techniques: through the transfer function and second-order distortion cancellation of the NMOS-PMOS pair, respectively. The mechanism of distortion canceling, through transfer function, is similar to noise cancelation since the distortion current can be modeled as a current source connected between the drain and source nodes. Based on the transfer functions, the output I_{M3} voltage due to M_2 and M_3 can be calculated and cancelled using balanced differential outputs. The effect of this distortion cancelation is degraded at high frequencies due to phase shift, which is also a problem in noise cancelation. The distortion from M_1 and M_4 cannot be cancelled by this method. In this case, the I_{M3} current originates from non-linear coefficients of M_1 and M_4. The parameters associated with the non-linear behavior can be simulated and show that the pMOS has a much lower 3rd-order non-linear coefficient, K_3, than that of the nMOS and therefore M_4 can be used as an auxiliary transistor, by adjusting its bias and size, in order to cancel the second order nonlinearity of the nMOS.

Through the techniques introduced above, the proposed LNA can achieve NF and gain comparable or better than those of reported inductorless LNA's requiring lower power consumption and supply voltage.

Chapter 6

6 MOSFET-Only Low Noise Amplifier with Double Feedback

6.1 Theoretical Analyses

In the MOSFET-only LNA with double feedback (Fig. 6.1), which is the proposed circuit, the load resistors are replaced by PMOS transistors, M_3 e M_4, operating in the triode region, which means these transistors behave, approximately, as linear resistors [7]. In order to enhance the gain, while maintaining a low noise figure, was decided apply a Double Feedback structure (DF), as shown in Fig. 6.1. This proposed circuit boosts the gain, and reduce the noise of M_1 that appears with the same level on the LNA outputs (load transistors M_3 e M_4), while the output signals remain balanced. This circuit is completely symmetrical, and therefore, is expected to achieve the best performance results.

In the feedback is used a high pass RC coupling. With these connections, the parasite capacitances of M_3 e M_4 will reduce the bandwidth (the gate-source and gate-drain capacitances), but the main goal is to achieve: high gain and low NF.

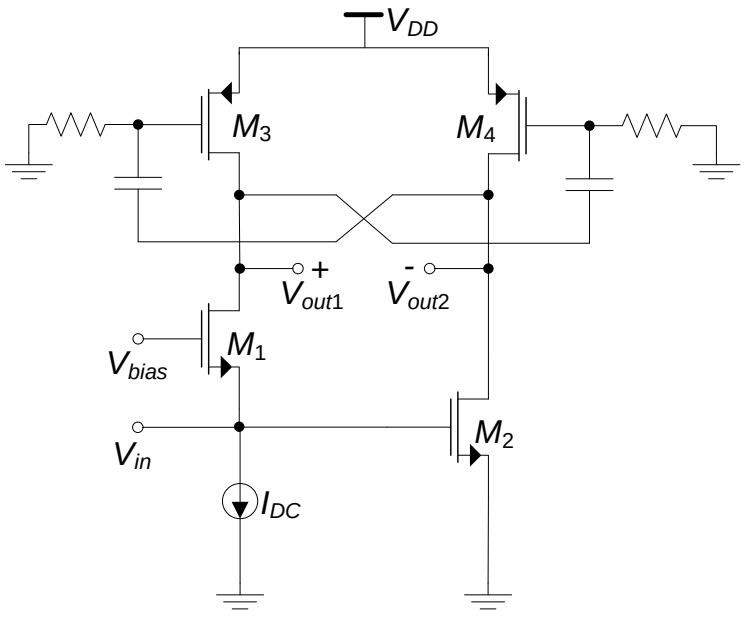

Figure 6.1- MOSFET-Only LNA with Double Feedback

To can obtain better results, we started by designing the circuit with 50 Ohm input matching. In order to get this, the transconductance gm_1 was imposed by first approach. After this, we had to balance the gain of the two stages by changing, mainly, the M_1 and M_2 dimensions. In the next section is shown the table with all the transistor´s dimensions.

Note that in the feedback structure is used a high pass RC coupling, as it can be seen in Fig. 6.1. With these connections, the parasites capacitances of M_3 and M_4 will neglect a little bit the bandwidth (the gate-source and gate-drain capacitances), but is obtained more gain and lower NF.

In order to provide some more circuit insight, were derived here the equations for gain (CG and CS stages) and LNA input impedance:

$$\frac{V_{out1}}{V_i} = \frac{g_{mCG}g_2 + g_{m2}g_{m3}}{g_1g_2 - g_{m3}g_{m4}}, \qquad (6.1)$$

$$\frac{V_{out2}}{V_i} = \frac{g_{m2}g_1 + g_{mCG}g_{m4}}{g_1g_2 - g_{m3}g_{m4}}, \qquad (6.2)$$

where, $g_1 = g_{ds1} + g_{ds3}$, $g_2 = g_{ds2} + g_{ds4}$ and $g_{mCG} = g_{m1} + g_{ds1}$.

Using equations (6.1) e (6.2), was obtained the LNA differential gain

$$A_v|_{Diff} = \frac{V_{out1} - V_{out2}}{V_i} \qquad (6.3)$$

$$\Leftrightarrow \quad A_v|_{Diff} = \frac{g_{mCG}(g_{m4} + g_2) + g_{m2}(g_{m3} + g_1)}{g_1g_2 - g_{m3}g_{m4}}. \qquad (6.4)$$

The input-impedance is given by

$$Z_{in} = \frac{g_1g_2 - g_{m3}g_{m4}}{g_{mCG}[g_2g_{ds3} - g_{m3}g_{m4}] - g_{m2}g_{m3}g_{ds1}}. \qquad (6.5)$$

Using the equations (6.4) and (6.5), is possible optimize the circuit performance in order to increase the gain, minimizing the impact in the input match.

From [24], in order to improve the noise figure, the g_{m2} should be greater than g_{m1}, while the g_{ds4} is increased to keep the output signals balanced.

$$g_{m2} = n \cdot g_{m1}$$

$$g_{ds4} = n \cdot g_{ds3}$$

The optimal value of n is obtained by simulation.

6.2 Simulations Results

The circuit prototype is designed using a 130 nm CMOS standard technology with 1.2 V supply. The circuit parameters are given on Table 1. The length of each transistor channel is the minimum (0.12 µm) to maximize speed, and V_{bias} is chosen to 815 mV to define the biasing current at the CS stage.

Table 1- MOSFET parameters

	I_D (mA)	W (µm)	r_{ds} (Ω)	g_{ds} (mS)	g_m (mS)
M_1	2	6.3	515.46	1.94	25.28
M_2	2.17	6.9	392.16	2.55	40.69
M_3	2	2.62	170.35	5.87	1.94
M_4	2.17	3.35	120.77	8.28	2.01

Note that the transistor's model for M_1 and M_2 was "N_12_RF" and for M_3 and M_4 was "P_12_RF".

Then, it will be shown a result of comparison between the theoretical and the simulated gain as show in Fig. 6.2. For the theoretical result was used equation 6.4 and the body effect was despised which makes the theoretical result is less than the simulated.

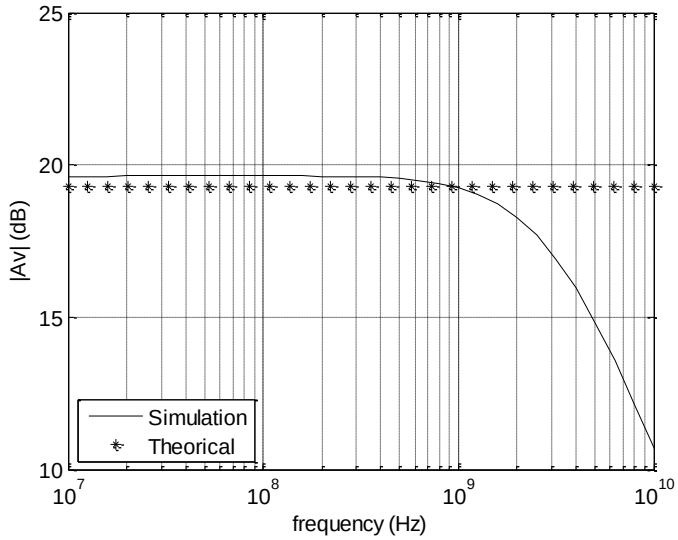

Figure 6.2- Comparison of Gain theoretical and simulated of LNA

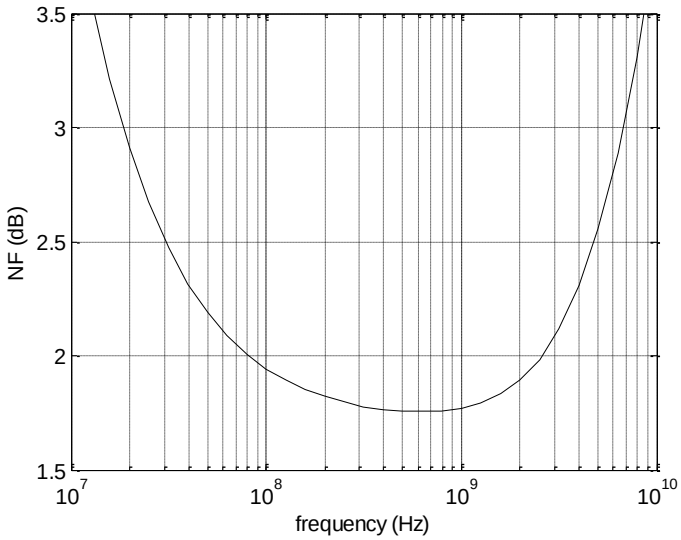

Figure 6.3- Noise Figure of LNA

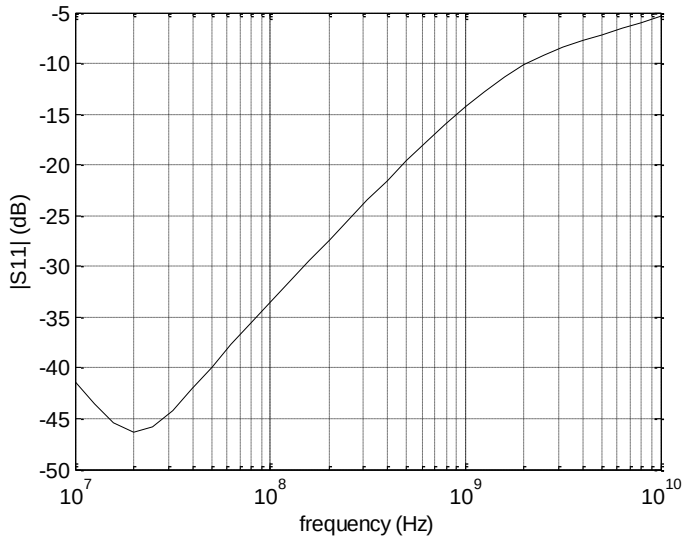

Figure 6.4- Input impedance of LNA

To estimate the LNA input matching is necessary to make a S-parameter analysis (Fig. 6.4). In theory the LNA is considered input matched if its $|S_{11}| < -10dB$, which means the bandwidth of 3 GHz for these designs. The LNA with Double Feedback with optimized gain has a better gain improvement over the traditional design, but has less bandwidth due to parasitics of the load transistors. In relation the NF was obtained less than 2 dB (Fig. 6.3), from 100 MHz up to 2.5 GHz.

Concerning linearity, Fig. 6.5 shows the simulated IIP3 for LNA with Double Feedback. It has an IIP3 above -5.5 dBm, which means that this design has poorer linearity, due to higher gain and by the intrinsic nonlinearities of MOSFET devices.

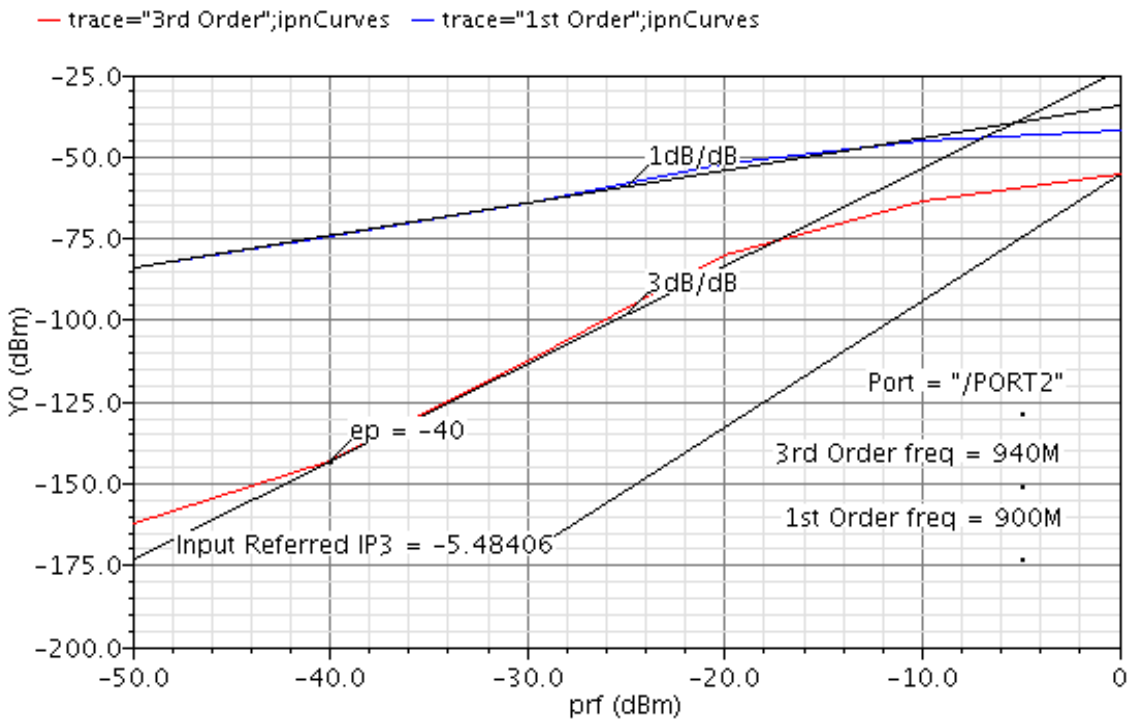

Figure 6.5- MOSFET-Only LNA with Double Feedback IIP3

It was decided employ a real current source, which will slightly reduce the gain, reduce the bandwidth, and increase the noise, and a Buffer (Fig. 6.6) to convert the differential outputs to the single-ended output, which reduced 6 dB in the Gain. The results are shown in the next subchapter.

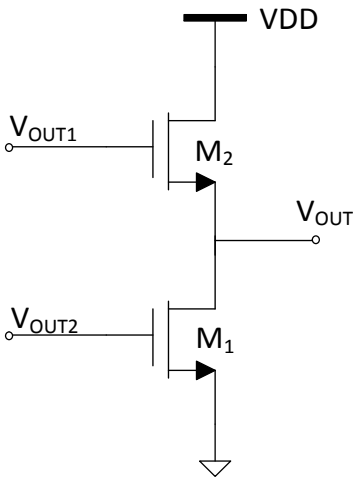

Figure 6.6- Balun of MOSFET-Only LNA with Double Feedback

6.3 Pre-Layout Simulations

In Fig. 6.7, 6.8 and 6.9 the simulation results for the complete circuit (LNA + Balun) are presented.

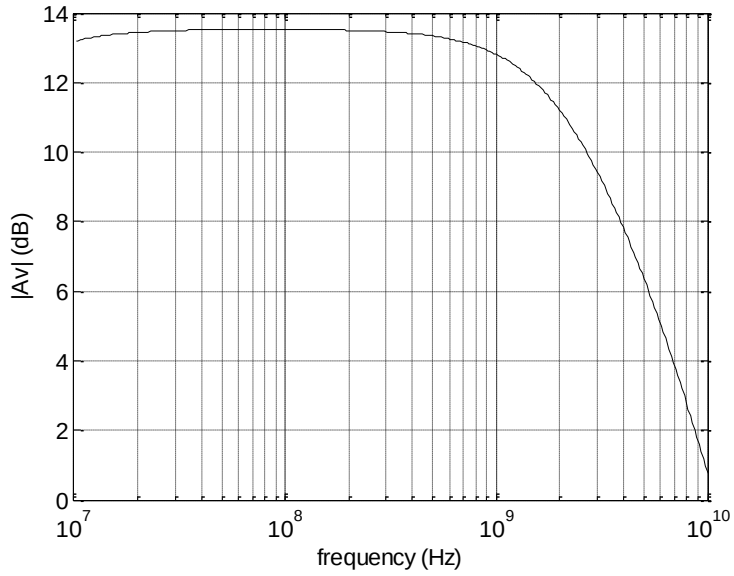

Figure 6.7- Gain of LNA

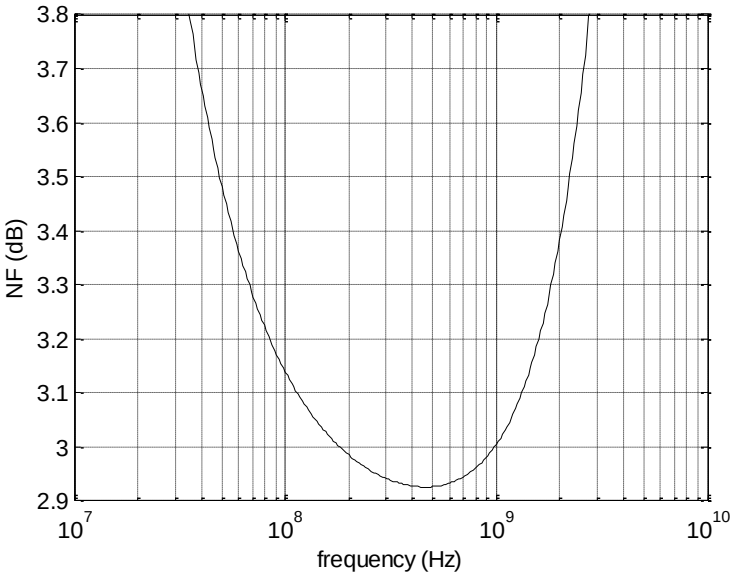

Figure 6.8- Noise Figure of LNA

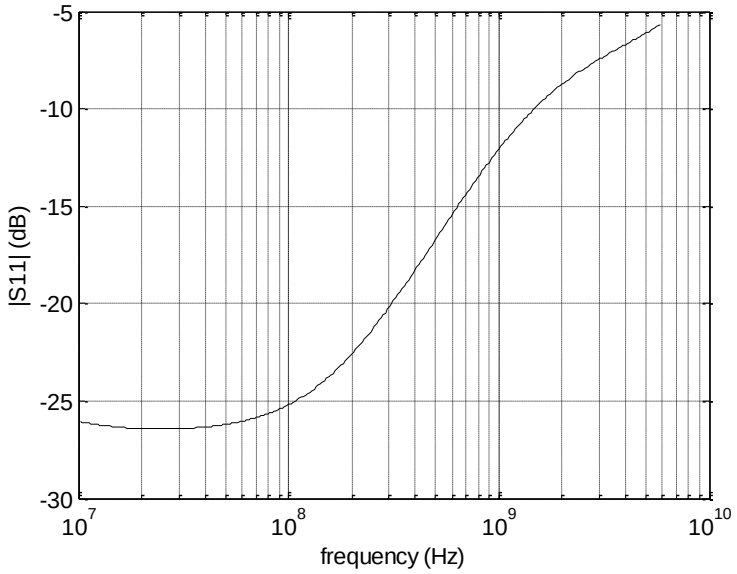

Figure 6.9- Input impedance of LNA

As we can see, the gain decreased about 6 dB mostly due to the buffer, the noise had a slightly increase and the bandwidth was reduced to 2.38 GHz. In relation to *IIP3*, it was obtained a better value, always bigger than 0 dB.

6.4 Layout Design And Post-Layout Simulations

Here is presented a circuit layout for the proposed MOSFET-Only Low Noise Amplifier with Double Feedback, and is performed a more realistic simulation including the RC parasitics. The results are compared with the schematic simulation results.

In Fig. 6.10 it is shown the MOSFET-Only Low Noise Amplifier with Double Feedback, which has a die area of $203.9 \times 132.2\,\mu m^2$ and in Fig. 6.11 is shown all the LNA circuit, which includes also Balun and real current source. The final circuit has a die area of $402.5 \times 341.4\,\mu m^2$. The technology used has constraints relative to the size and the maximum number of gate fingers for RF MOSFETs (more gate fingers leads to less gate resistance, therefore minimizing the effect of the parasitics). The V_{bias} is tuned to approach the currents for M_2 and M_4.

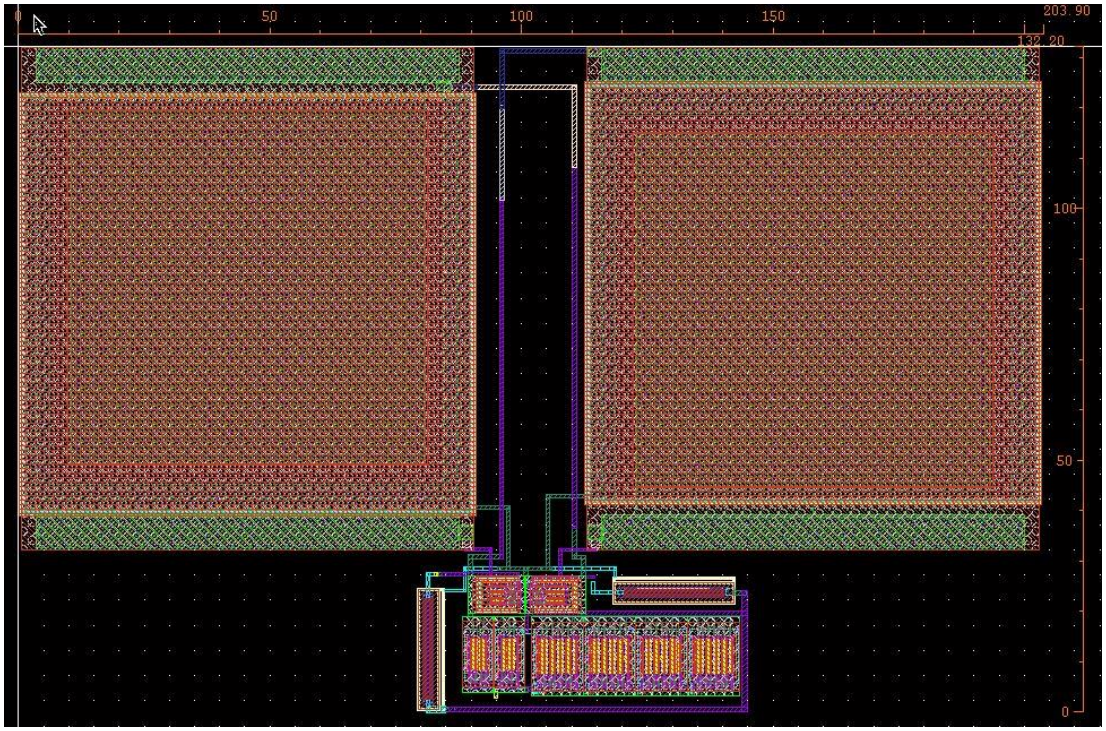

Figure 6.10- MOSFET-Only LNA layout (203.9 × 132.2 μm^2)

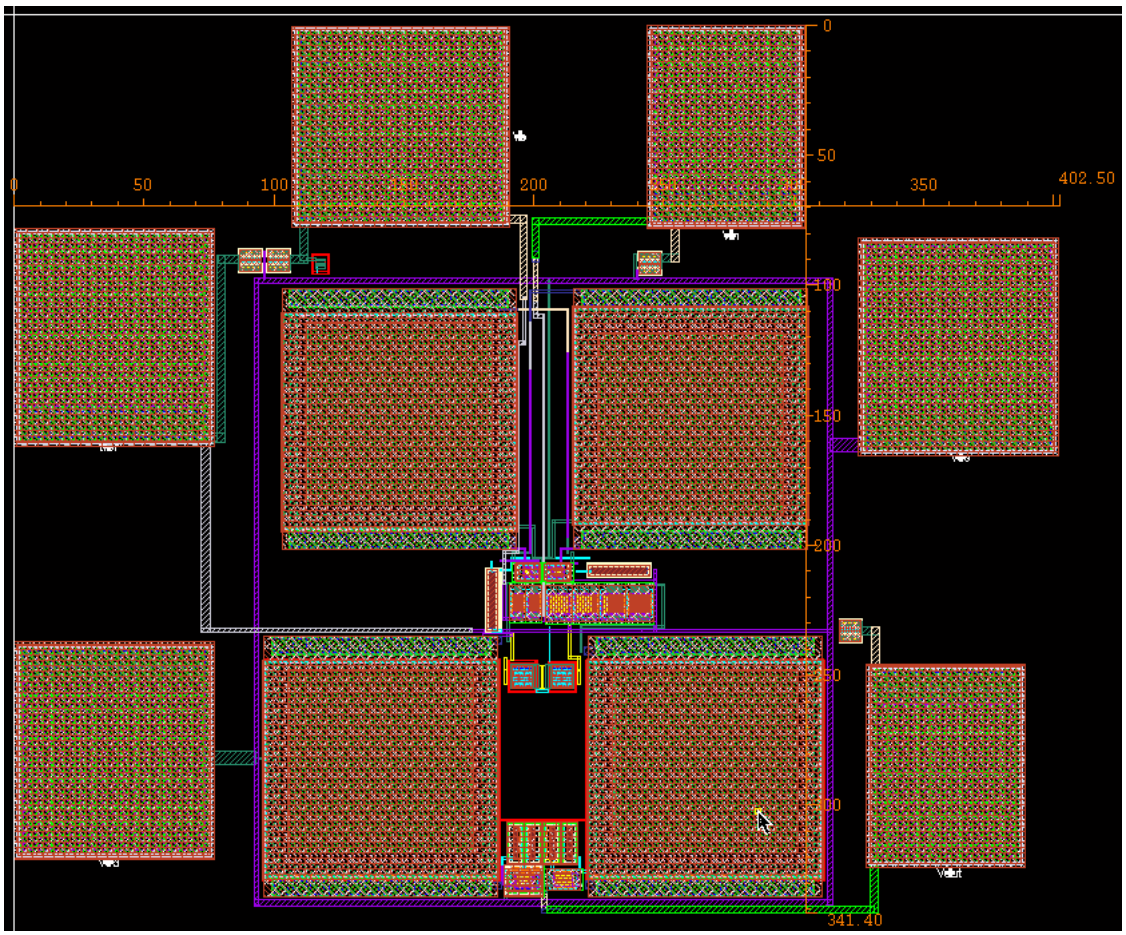

Figure 6.11- Layout of the total circuit with real current source, Balun and Pads (402.5 × 341.4 μm^2).

The post-layout simulation results for the proposed LNA are shown in Figs. 6.12, 6.13 and 6.14.

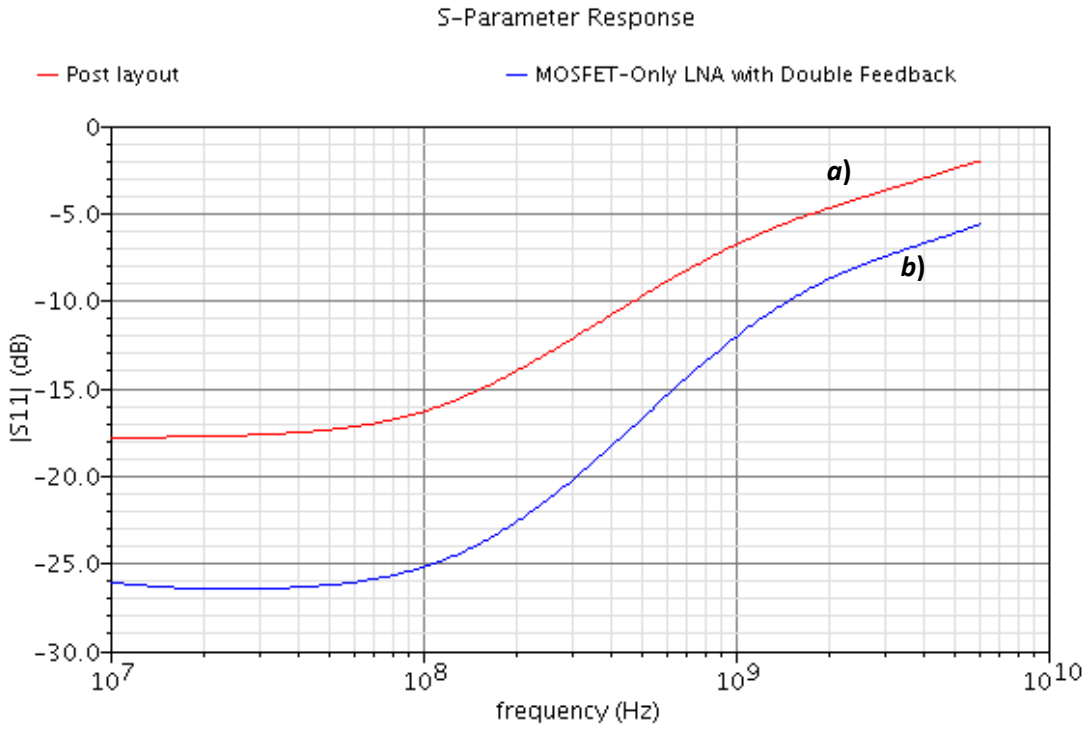

Figure 6.12- Input impedance ((a) Schematic, (b) Post-layout)

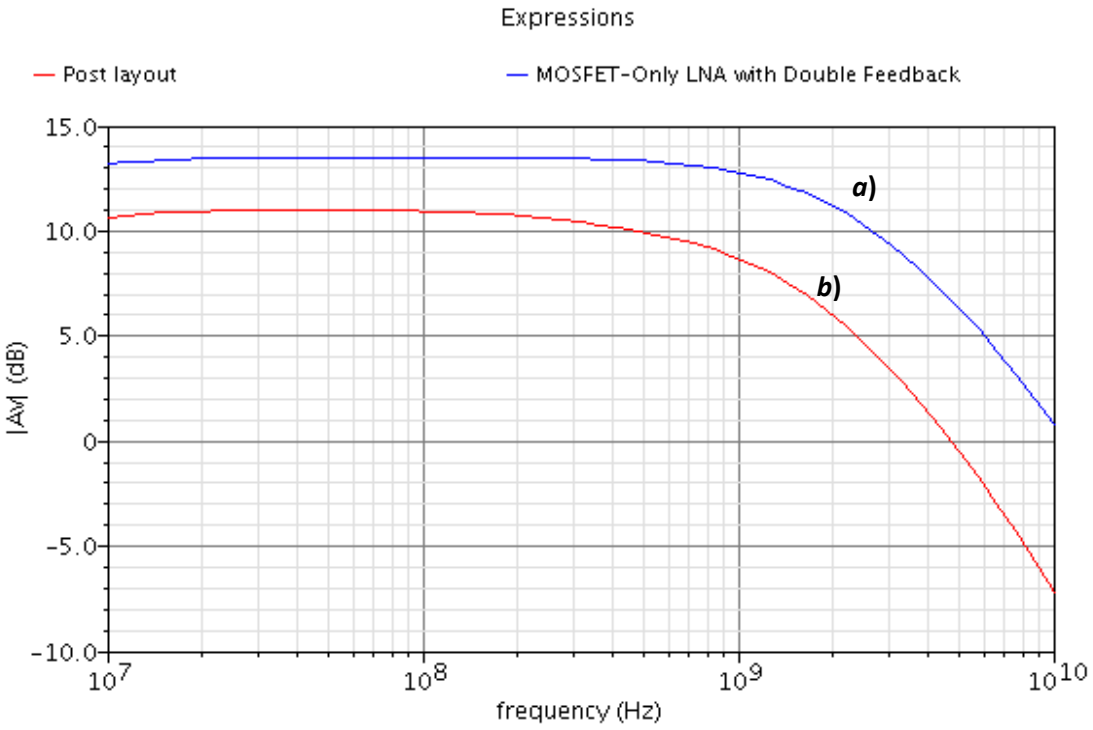

Figure 6.13- Gain ((a) Schematic, (b) Post-layout)

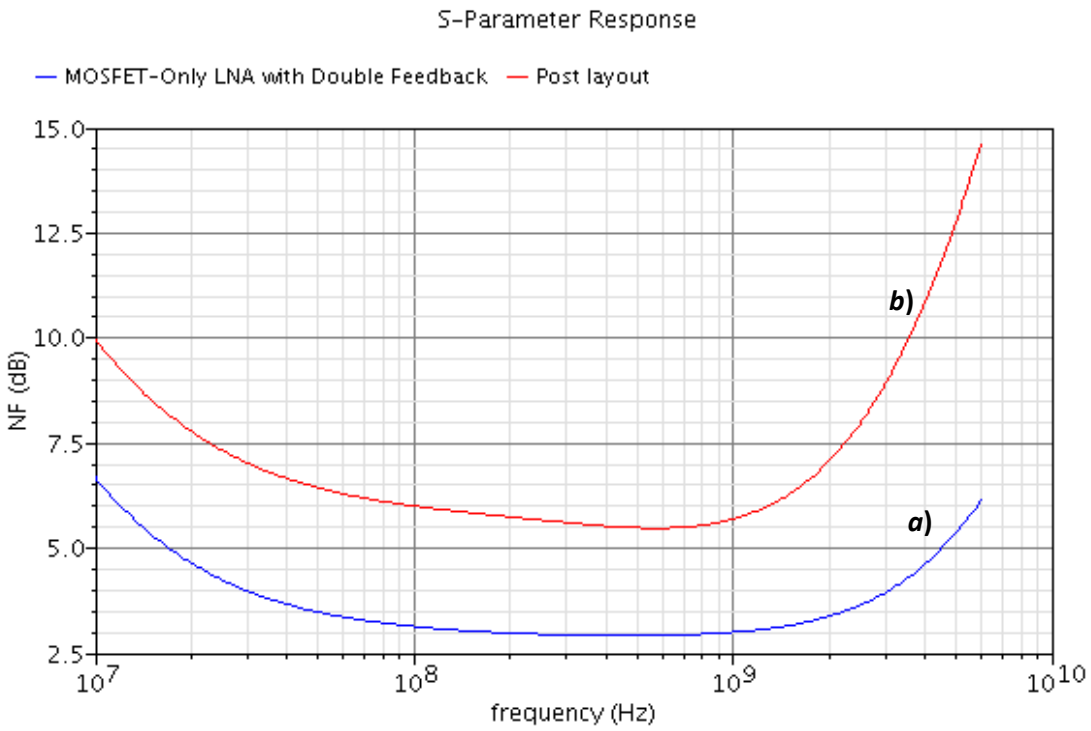

Figure 6.14- Noise Figure ((a) Schematic, (b) Post-layout)

The post-layout simulations show the input matching (Fig. 6.12) is a bit affected (approximately 3.5 dB), which means the bandwidth is smaller. The gain decreases and in relation to the NF, it increases by approximately 3 dB, due to the thermal noise of M_1 being not fully canceled.

6.5 Discussion

For a better comparison of the obtained results, the following figure of merit is used [26]:

$$FOM = \frac{Band[GHz].A_v[lin].IIP3[mW]}{Power[mW].(NF-1)} \qquad (6.6)$$

Table 2- Comparison with state-of-the art LNAs

Ref	**Tech (nm)**	***Band* (GHz)**		**$\|A_V\|$ (dB)**	***NF* (dB)**	***IIP3* (dBm)**	***Power* (mW)**	***FOM***
[23]	65	0.2	5.2	15.6	< 3.5	0	14	1.74
[27]	90	0.5	8.2	25	< 2.6	-4	42	1.58
[28]	90	0.8	6	20	< 3.5	-3.5	12.5	1.50
[29]	130	0.2	3.8	11.2	< 2.85	-2.7	1.9	3.98
[30]	180	0.5	0.9	16	< 4.3	-1.5	22	0.05
[31]	180	0.1	0.9	15	< 4.2	2.6	10	0.50
[7]	130	0.2	5	20.4	< 2.6	-10.9	4.8	1.04
This work	130	0.1	3.38	19.65	< 2.17	-4.92	5	3.13

Comparing the results of proposed LNA, before having the buffer and the real current source, with the state-of-the-art Inductorless LNAs (Table 2) can be conclude that the proposed circuit has the advantages in gain and noise figure. This circuit presents one of the highest gain and one of the lowest NF. In relation to FOM, we can verify that the circuit present a high FOM when it is compared with the others. The drawbacks are a little reduction of bandwidth and the decrease of a circuit non-linearity, (reduction of *IIP3*) when it is compared with the LNA with resistors. Note that we have worse FOM than in [29], because it presents a very low gain, when compared with this work.

Chapter 7

7 Conclusions and Future Work

7.1 Conclusions

The main goal of this thesis was to present a low voltage and low power wideband balun LNA, which was based on the combination of a common-gate and a common-source sage, with double feedback structure dimensioned for high gain and low NF. It was derived equations for the gain and input matching, which were validated through simulations. A circuit prototype operating at 1.2 V is presented in a 130 nm CMOS technology, which validates the proposed methodology.

Simulation results show that the gain of the balun LNA is 19.65 dB, and the NF is below 2.17 dB for a power consumption of 5 mW. The proposed circuit is especially useful for low power and low voltage operation in biomedical applications (ISM and WMTS bands).

The proposed circuit, with 1.2 V supply, to the best of the authors' knowledge, has one of the high FOM (3.13 mW^{-1}) when compared with CMOS LNAs in the literature.

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7.2 Future Work

As future work, we can:

- ✓ A complete theoretical characterization of noise and linearity of the circuit;
- ✓ Implement a circuit prototype operating at 0.6 V, replacing the MOS by DTMOS;
- ✓ Validate the results by measurements on a test-circuit;
- ✓ Integrate our LNA in a low-voltage CMOS receiver.

Appendix A

Published Paper

A 1.2 V Low Noise Amplifier with Double Feedback for High Gain and Low Noise Figure

A 1.2 V Low Noise Amplifier with Double Feedback for High Gain and Low Noise Figure

I. Bastos, F. Querido, D. Amoêdo, L. B. Oliveira,
J. P. Oliveira and J. Goes

Manuel M. Silva
INESC-ID Lisboa
Tech. University of Lisbon
Lisbon, Portugal
manuel.silva@inesc-id.pt

CTS-UNINOVA, Dep. Eng. Electrotécnica, Faculdade de Ciências e Tecnologia,
Universidade Nova de Lisboa
Caparica, Portugal
bastos356@gmail.com, l.oliveira@fct.unl.pt

Abstract. In this paper we present a balun low noise amplifier (LNA) in which the gain is boosted using a double feedback structure. The circuit is based in a conventional Balun LNA with noise and distortion cancellation. The LNA is based in two basic stages: common-gate (CG) and common-source (CS). We propose to replace the resistors by active loads, which have two inputs that will be used to provide the feedback (in the CG and CS stages). This proposed methodology will boost the gain and reduce the NF. Simulation results, with a 130 nm CMOS technology, show that the gain is 23.8 dB and the NF is less than 1.8 dB. The total power dissipation is only 5.3 (since no extra blocks are required), leading to an FOM of 5.7 mW^{-1} from a nominal 1.2 supply.

Keywords: CMOS LNAs, Noise canceling, Wideband LNA.

1 Introduction

Nowadays, there is a high demand for wireless communications, which includes Industrial, Scientific, and Medical (ISM) and Wireless Medical Telemetry Service (WMTS) applications [1]. These low cost applications require low power, low voltage transceivers fully integrated in a single chip [2-4]. The LNA that is a key block in these systems will be investigated in this paper.

Wideband LNAs with high gain and low noise figure (NF), using noise and distortion cancelation have been proposed [5-7]. But, these circuits have large power dissipation for high gain and low noise figure.

In this paper our main goal is to design a very low area and low cost LNA, with very high gain and low NF using a 1.2 V supply. This is obtained by replacing the load resistors by transistors biased close to saturation. In [7] a circuit operating at 1.2

V with controllable gain was proposed. In this paper we investigate the possibility of introduce a double feedback technique to boost the gain and reduce the noise figure (NF).

Equations for gain and noise figure are presented, which can be used to optimize the circuit performance. A circuit prototype in a 130 nm standard CMOS technology at 1.2 V have been designed and simulated to demonstrate the proposed technique.

The circuit prototype has gain of 23.8 dB and NF below 2 dB, dissipating only 5.3 mW, leading to a FOM of 5.7 mW^{-1}, which is, to the authors' knowledge, the best FOM in the literature for LNAs with a nominal 1.2 V supply.

2 Contribution for Internet of Things

Recently, more devices are being embedded with sensors and actuators with the ability to communicate and exchange information, creating a cloud environment. The physical communication plays a critical role in portable wireless devices equipped with transceivers where power consumption, immunity to noise, and signal amplification are important parameters to ensure a reliable and efficient communication in a crowded channel environment. With this goal in mind the design of RF front-end blocks for low power applications, in CMOS technology, will contribute towards the achievement of more cheap and robust devices. In this paper we will focus on the design of low power LNAs.

3 Balun LNA with Noise Cancellation

In a receiver path, since typically, the antenna and RF filters are single-ended, it is very important to have a LNA with single-ended configuration input. A differential signal in the receiver is preferred to reduce harmonic distortion and to reject power supply and substrate noise [6]. Traditionally, we have an external balun that converts single-ended signals to differential, but it introduces losses and degrades the receiver NF. A balun LNA is a very good solution to convert a single-ended to a differential signal, which simplifies the design avoiding the external balun [6].

A balun LNA, in which the thermal noise of CG-transistor is canceled because this noise appears in phase at two outputs and their gains are in opposition, is proposed in [6]. The gain is doubled and the noise is reduced when the output signals are balanced. It can also be shown that the distortion introduced by M_1 is also cancelled.

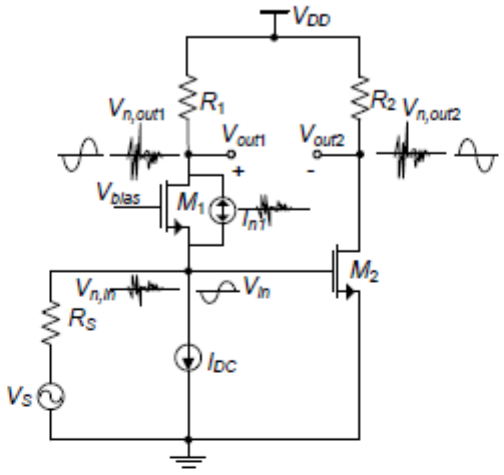


Fig. 1. Balun LNA with noise canceling of CG-transistor [6].

The differential voltage gain of the LNA is obtained from the difference of the common-gate (CG) stage and the common-source (CS) stage gains:

$$A_v|_{Diff} = g_{m1}(R_1//r_{ds1}) + g_{m2}(R_2//r_{ds2}) . \quad (1)$$

where, r_{ds} is the transistors output resistance and g_m is the transconductance.

The input inpedance is given, approximately:

$$Z_{in} = \frac{1}{g_{m1}} . \quad (2)$$

Note that the body and source of M_1 are connected to eliminate the body effect.

4 Proposed Circuit

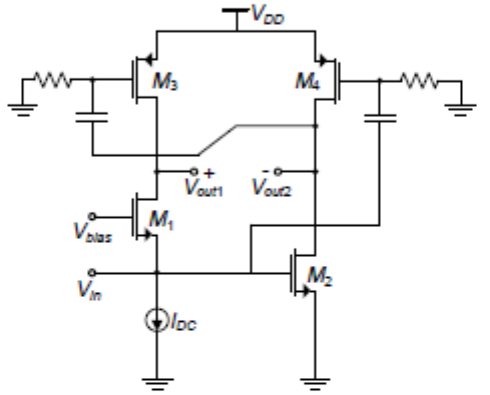
Considering the traditional CG-CS LNA circuit (Fig. 1) as reference, we investigate a topology using active loads, by replacing the resistors by transistors, biased in the triode region, which behave, approximately, as linear resistors [7]. In order to enhance the gain, while maintaining a low noise figure, we investigate first the possibility to use local Feedforward and Feedback (FF), as shown in Fig. 2 a).

Taking the advantage of using transistors, instead of resistors, we apply V_{in} on the gate of transistor to the gate of M_4, which is amplified and added to V_{out2}. The resulting signal is amplified through M_3 by feedback and added to V_{out1}. With this structure we have a significant increase in the gain, mainly in the CG stage, which need to be carefully designed to ensure 50 Ohms input match. In this case the thermal noise of M_1 is only partially cancelled, which degrades the LNA noise figure. To

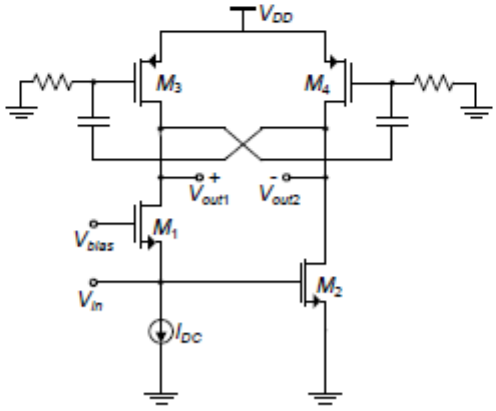
overcome this issue we propose a new circuit approach in which we apply a Double Feedback structure (DF), as shown in Fig. 2 b).

This proposed circuit boost the gain, and reduce the noise of M_1 that appears with the same level on the LNA outputs (load transistors M_3 and M_4), while the output signals remain balanced. This circuit is more simply and completely symmetrical, and therefore, is expected to achieve the best performance results.

In the feedback is used a high pass RC coupling, as shown in Fig. 2. With these connections, the parasites capacitances of M_3 and M_4 will reduce the bandwidth (the gate-source and gate-drain capacitances), but the main goal is achieved: high gain and low NF.



a)



b)

Fig. 2.a) LNA using FF. **b)** Proposed LNA using DF.

In order to provide some circuit insight, we derive here the equations for gain (CG and CS stages) and LNA input impedance (for the proposed DF case):

$$\frac{V_{out1}}{V_{in}} = \frac{g_{mCG}g_2 + g_{m2}g_{m3}}{g_1 g_2 - g_{m3}g_{m4}} . \quad (3)$$

$$\frac{V_{out2}}{V_{in}} = -\frac{g_{m2}g_1 + g_{mCG}g_{m4}}{g_1 g_2 - g_{m3}g_{m4}} . \quad (4)$$

where,

$$g_1 = g_{ds1} + g_{ds3} .$$

$$g_2 = g_{ds2} + g_{ds4} .$$

Using (3) and (4), we obtain the LNA differential gain,

$$A_v|_{Diff} = \frac{V_{out1} - V_{out2}}{V_{in}} = \frac{g_{mCG}(g_{m4} + g_2) + g_{m2}(g_{m3} + g_1)}{g_1 g_2 - g_{m3}g_{m4}} . \quad (5)$$

The input-impedance is given by

$$Z_{in} = \frac{g_1 g_2 - g_{m3}g_{m4}}{g_{mCG}[g_2 g_{ds3} - g_{m3}g_{m4}] - g_{m2}g_{m3}g_{ds1}} . \quad (6)$$

Using equations (5) and (6), we can optimize the circuit performance in order to increase the gain, minimizing the impact in the input match.

From [6, 7], if it is assumed that $g_{m1} = g_{m2} = g_m$, the noise factor is:

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha_f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} . \quad (7)$$

where k is Boltzmann's constant, c_{ox} is the oxide gate capacitance per unit area, W_i and L_i are the transistor dimensions, T is the absolute temperature, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depend on the size of the transistors [8, 9]. With the proposed circuit there is additional noise due to the double feedback structure, however, this can be minimized by proper design.

From [6], to improve the noise figure, the g_{m2} should be greater than g_{m1}, while the g_{ds4} is increased to keep the output signals balanced.

$$g_{m2} = n \cdot g_{m1} .$$

$$g_{ds4} = n \cdot g_{ds3} .$$

The optimal value of n is obtained by simulations.

5 Simulation Results

The circuit prototype is designed using a 130 nm CMOS standard technology with 1.2 V supply. The circuit parameters are given on Table 1. The length of each

transistor channel is the minimum to maximize speed, and V_{bias} is defined in 760 mV to define the biasing current at the CS stage.

Table 1. LNA circuit parameters using DF.

	I_D (mA)	$\overline{W}$ (μm)	r_{ds} (Ω)	g_{ds} (mS)	g_m (mS)
M_1	2	139.2	472	2.12	30.80
M_2	2.43	358.4	357	2.80	44.23
M_3	2	13.14	236	4.23	2.07
M_4	2.43	16.4	186	5.38	2.48

In Table 2 we compare the theoretical results with simulations. We use equation (1) to traditional LNA with resistors [6] and using MOS in triode [7], and equation (5) for the proposed DF approach.

Table 2. Gain (dB) for different topologies.

	Res	*MOS*	*DF*
Theoretical	19.07	20.45	23.78
Simulation	19.03	20.50	23.81

In Table 3 we compare the simulation results for the traditional case with resistors, MOS transistors, and two approaches capable to boost the gain: 1) using feedback and feedforward (FF), and 2) the proposed case of double feedback (DF).

In order to investigate the influence of double feedforward in the LNA key parameters: gain, noise figure, linearity, and frequency band, several simulations are presented in Table 3. For a better comparison of the obtained results, the following figure of merit is used [10]:

$$\text{FOM}[\text{mW}^{-1}] = \frac{Gain}{(NF-1)P_{DC}[\text{mW}]}. \quad (8)$$

Table 3. Circuit Simulations for different topologies.

	Gain (dB)	*NF* (dB)	*IIP3* (dBm)	*Power* (mW)	*Band* (GHz)	*FOM* (mW^{-1})
Res	19.03	< 2.34	3.62	5.16	0.2-7.4	2.43
MOS	20.50	< 2.02	-3.47	5.30	0.2-6	3.37
FF	23.28	< 2.39	-11.03	5.51	0.1-2.5	3.61
DF	23.81	< 1.79	-9.92	5.32	0.1-2	5.72

In Table 3 is shown that the DF approach has the highest gain and the lower NF, leading to the highest FOM. The disadvantages are the increase of the circuit non-linearity and the reduction of the available bandwidth.

In figs. 3 to 5, the simulation results for the input match (S11), gain, and NF, for the proposed circuit (DF) are presented.

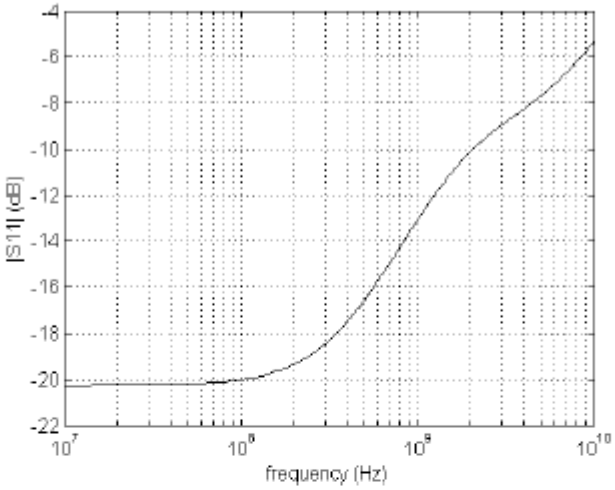


Fig. 3. Simulated LNA S11 parameter.

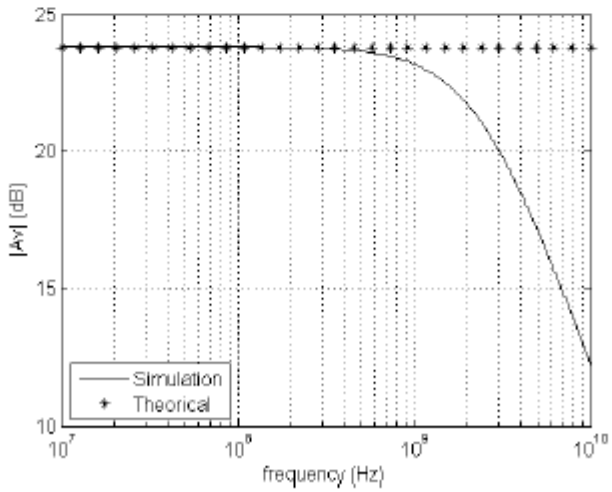


Fig. 4. Simulated LNA Gain.

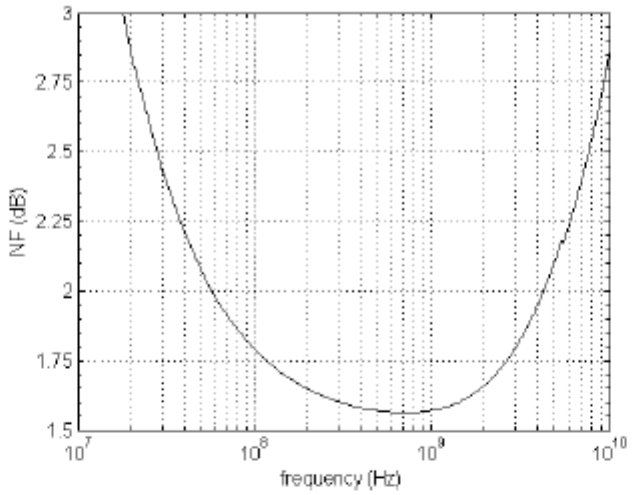


Fig. 5. Simulated LNA Noise Figure.

Comparing these results with state-of the art inductorless LNA (table 4), we observe that our circuit is very good in terms of gain and NF, and has very low power, which leads to the best FOM (please note that the results are obtained by simulation, some degradation is to be expected in the fabricated circuit; some of the references in table 4 are from measurements).

Table 4. Comparison with state-of-the art LNAs.

Ref	Tech (nm)	Band (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FOM (mW^{-1})
[6]^{M}	65	0.2-5.2	13-15.6	< 3.5	>0	14	0.4
[11]^{M}	90	0.5-8.2	22-25	< 2.6	-4/-16	42	0.5
[12]^{M}	90	0.8-6	18-20	< 3.5	>-3.5	12.5	0.6
[13]^{S}	90	0.1-1.9	20.6	< 2.7	10.8	9.6	1.3
[14]^{S}	130	0.2-3.8	11.2	< 2.8	-2.7	1.9	2.1
[15]^{M}	180	0.5-0.9	16	< 4.3	-	22	0.2
[16]^{M}	180	0.1-0.9	15	< 4.2	-	10	0.3
[7]^{S}	130	0.2-5	20.4	2.6	-10.9	4.8	2.7
[17]^{S}	130	0.2-6.6	19.8	< 1.8	1.6	4.8	3.5
This Work^{S}	**130**	**0.1-2**	**21.7-23.8**	**1.6-1.8**	**-9.7**	**5.3**	**5.7**

(^{S}) - Simulation results. (^{M}) - Measurement results.

The proposed circuit approach is especially interesting in low power and low voltage biomedical applications [1]. Since in these applications low power is the key aspect and some non-linearity can be tolerated. There are ISM bands in 450 MHz and 900 MHz and WMTS band in 600 MHz and 1.4 GHz, for which this circuit can be a good alternative to the conventional solutions.

6 Conclusions

In this paper we present a low voltage and low power wideband balun LNA with DF for high gain and low NF. A circuit prototype operating at 1.2 V is presented in a 130 nm CMOS technology, which validates the proposed methodology. Simulation results show that the gain of the balun LNA is 23.8 dB, and the NF is below 2 dB for a power consumption of 5.3 mW. The proposed circuit is especially useful for low power and low voltage operation in biomedical applications (ISM and WMTS bands).

The proposed circuit, with 1.2 V supply, to the best of the authors' knowledge, has the high FOM (5.7 mW^{-1}) when compared with CMOS LNAs in the literature.

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